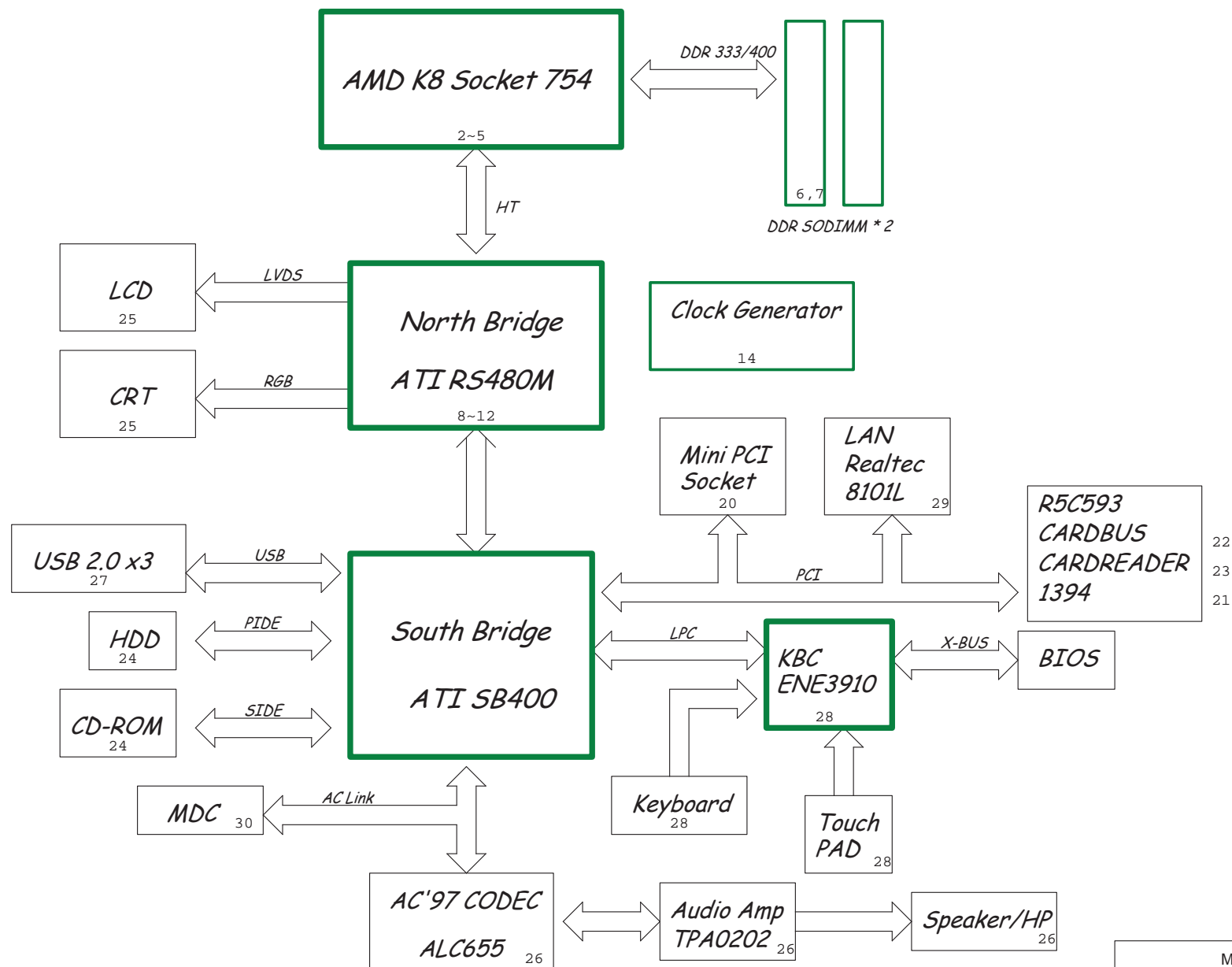




MS-1013 Ver:0C



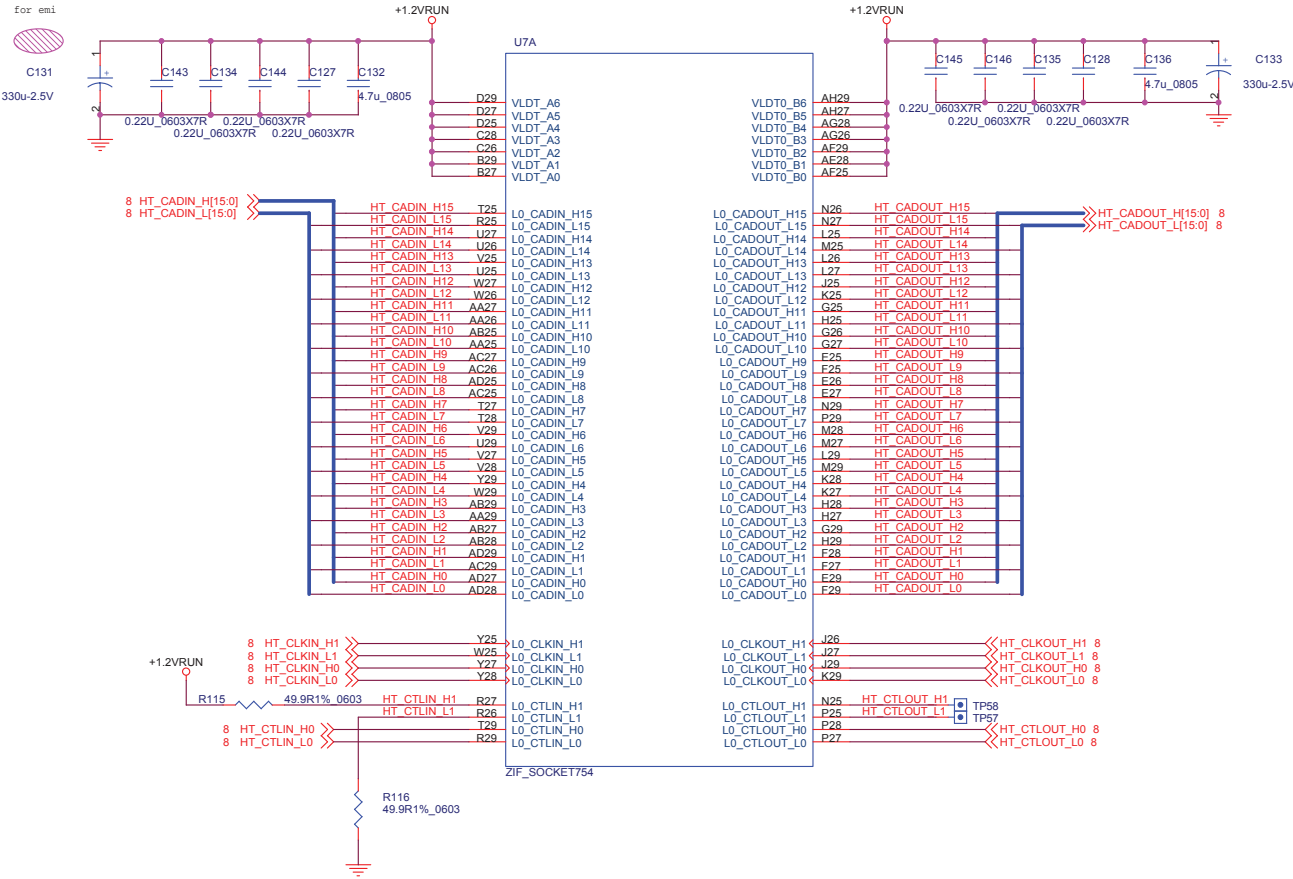
Clawhammer HT Interface

LAYOUT: Place HT bypass caps on topside
near unconnected Clawhammer HT Link

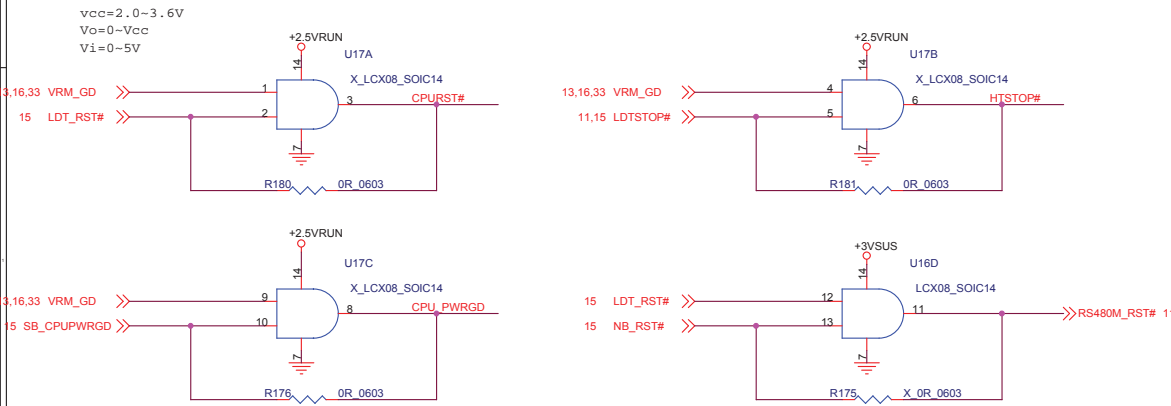
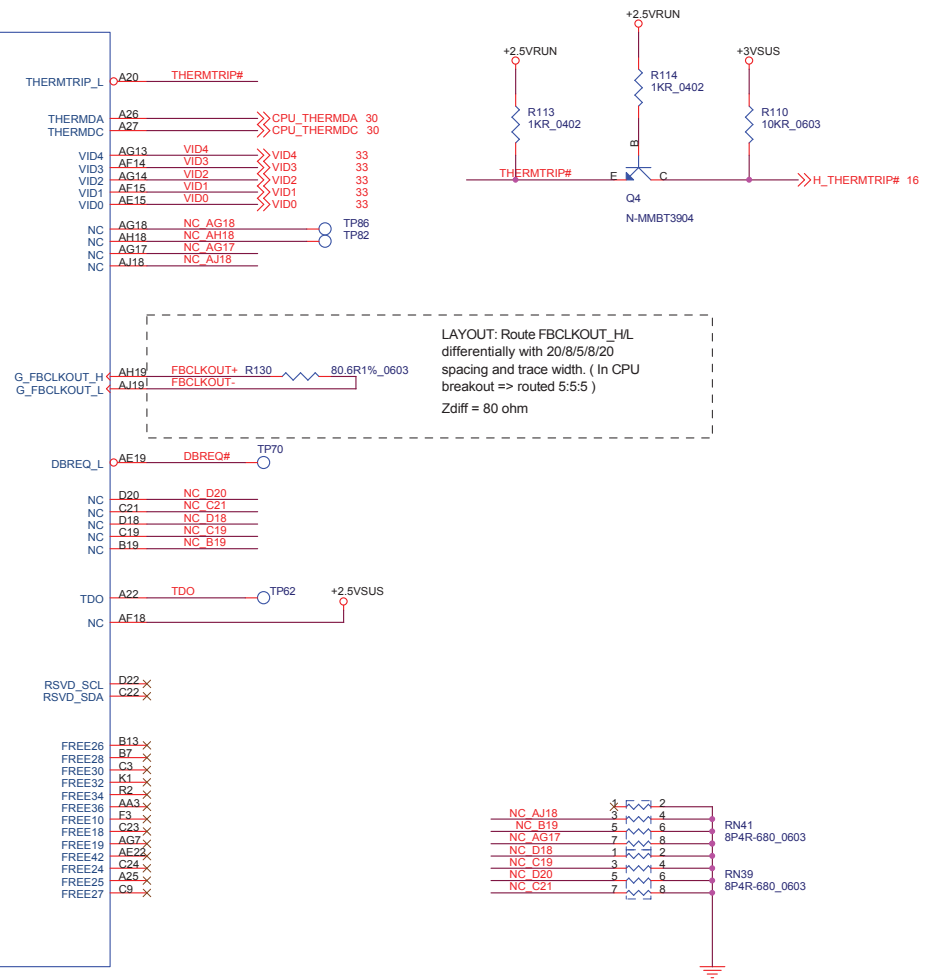
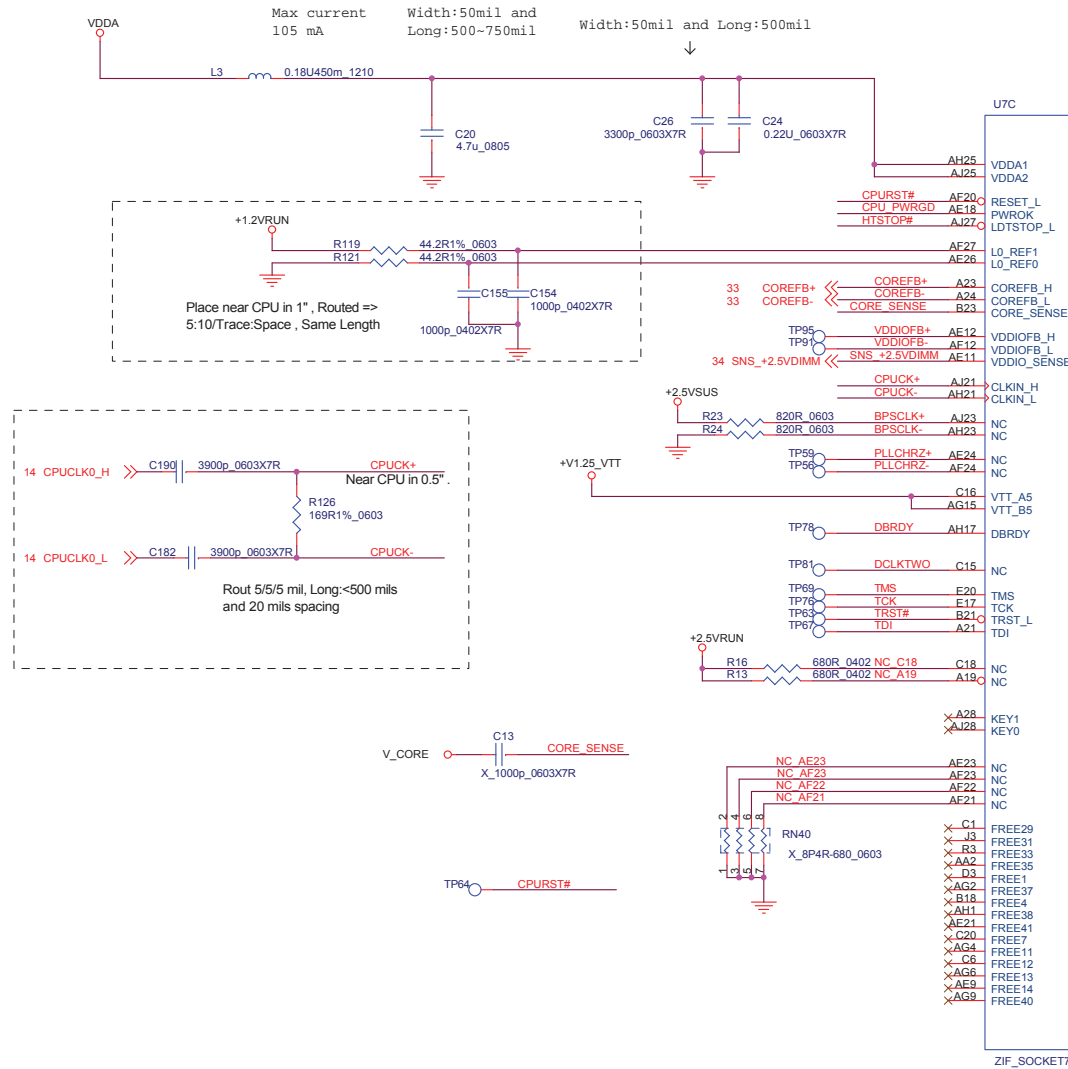
VLDT Power Decoupling

VLDT Plane Rout with 250 mil trace or a plane

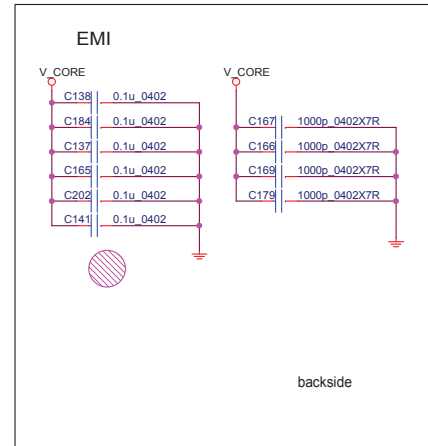
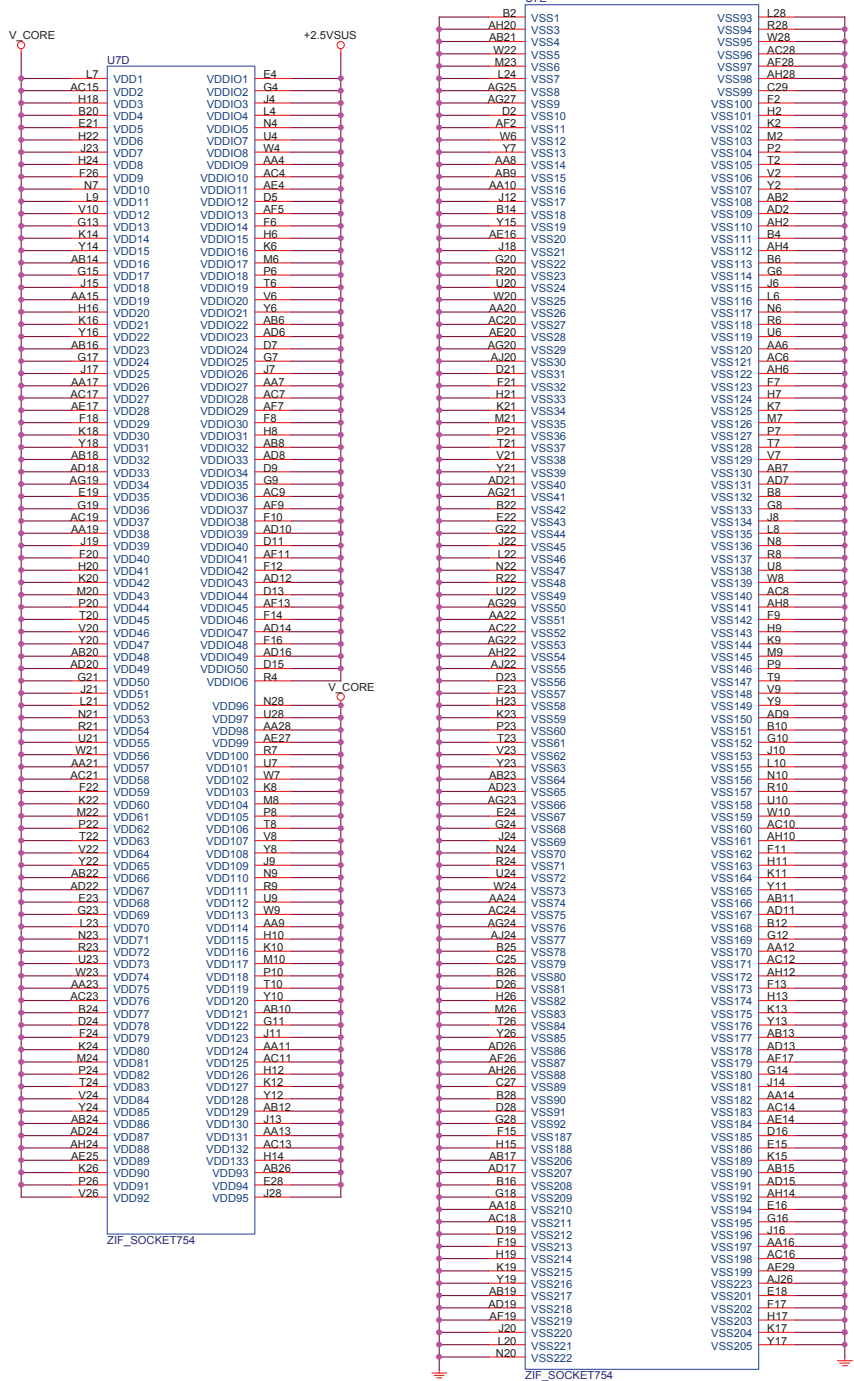
VLDT plane In CPU pins rout >100 mil



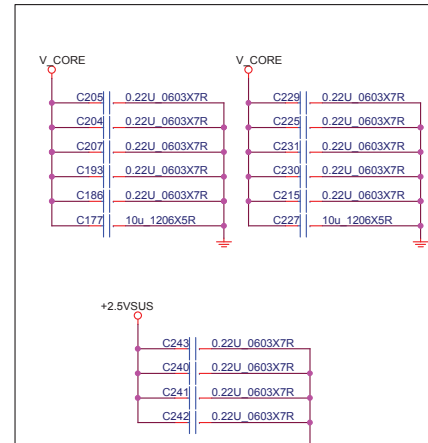
Clawhammer Control and Debug



Clawhammer Power and Ground Connections

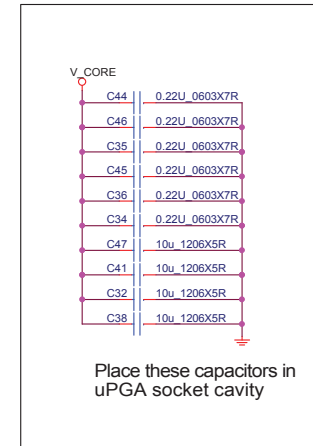


backside

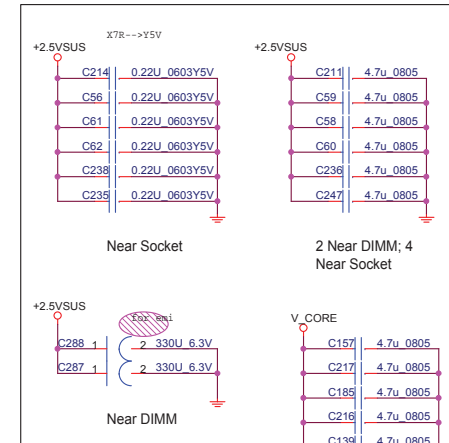


backside

Place these decoupling capacitors on solder layer of processor

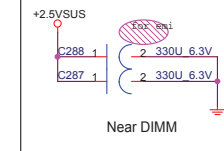


Place these capacitors in uPGA socket cavity



Near Socket

2 Near DIMM; 4 Near Socket

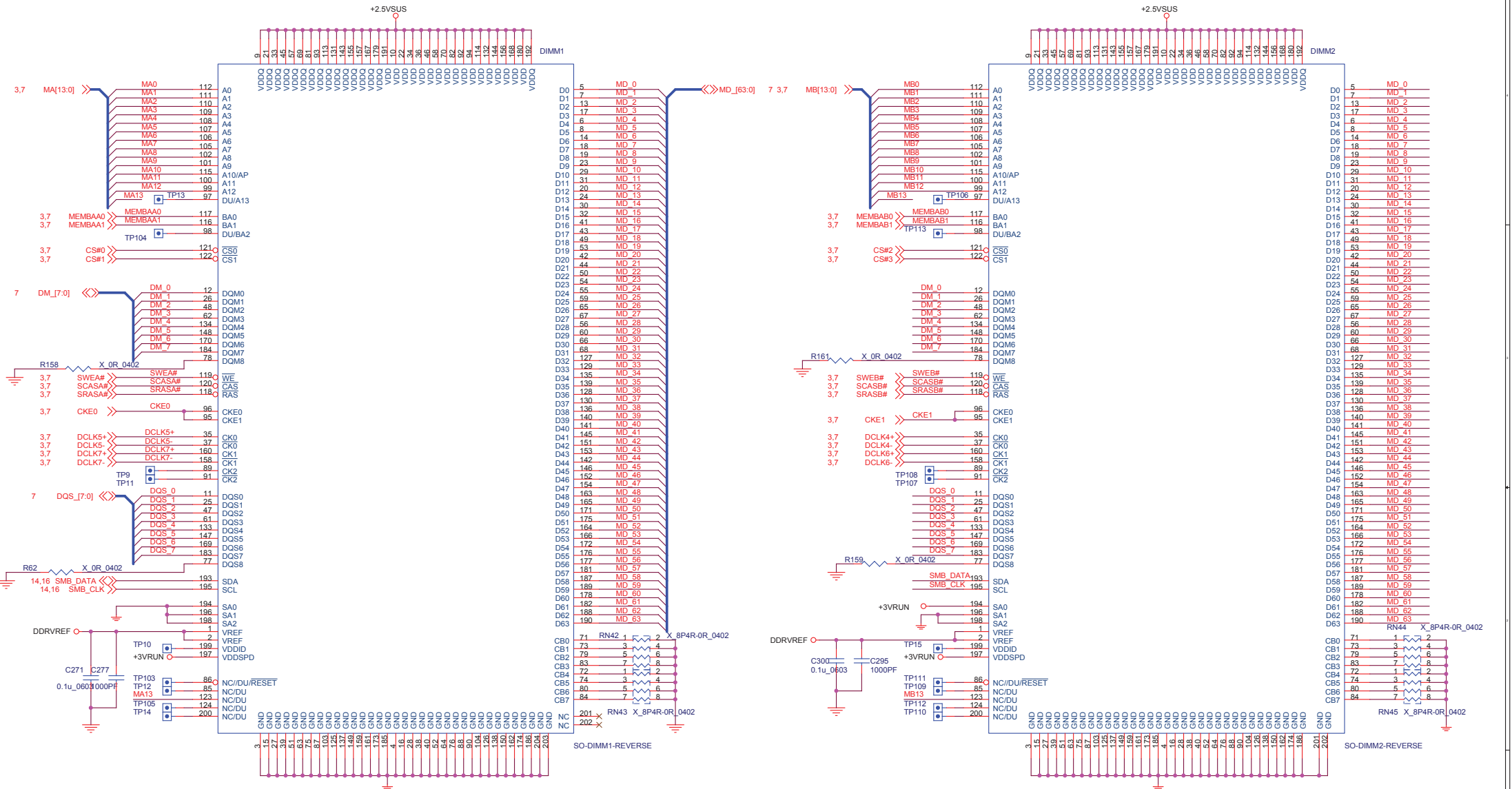


Near DIMM

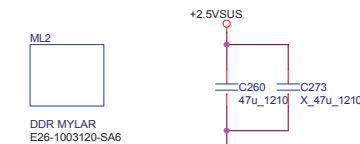
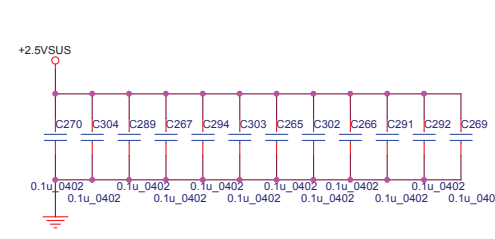
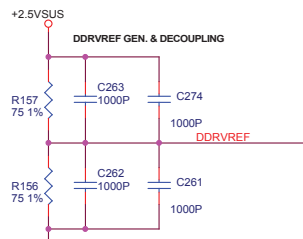
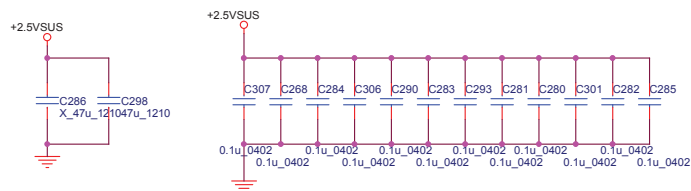
Close to socket

Place these capacitors near socket

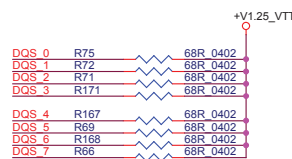
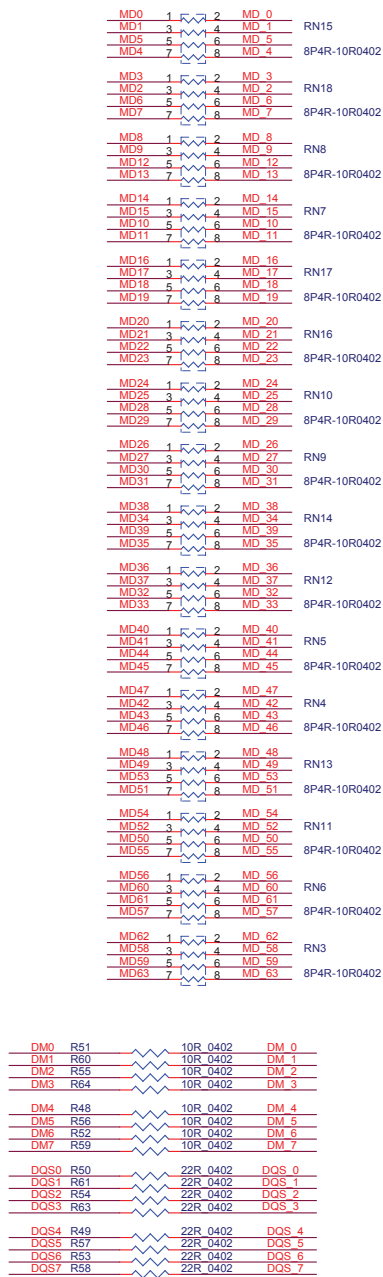
Unbuffered DDR333 SODIMM Sockets



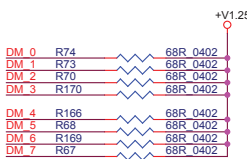
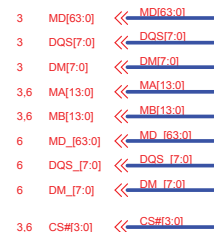
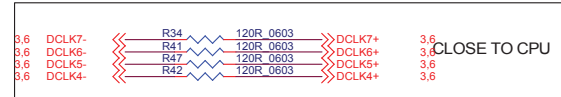
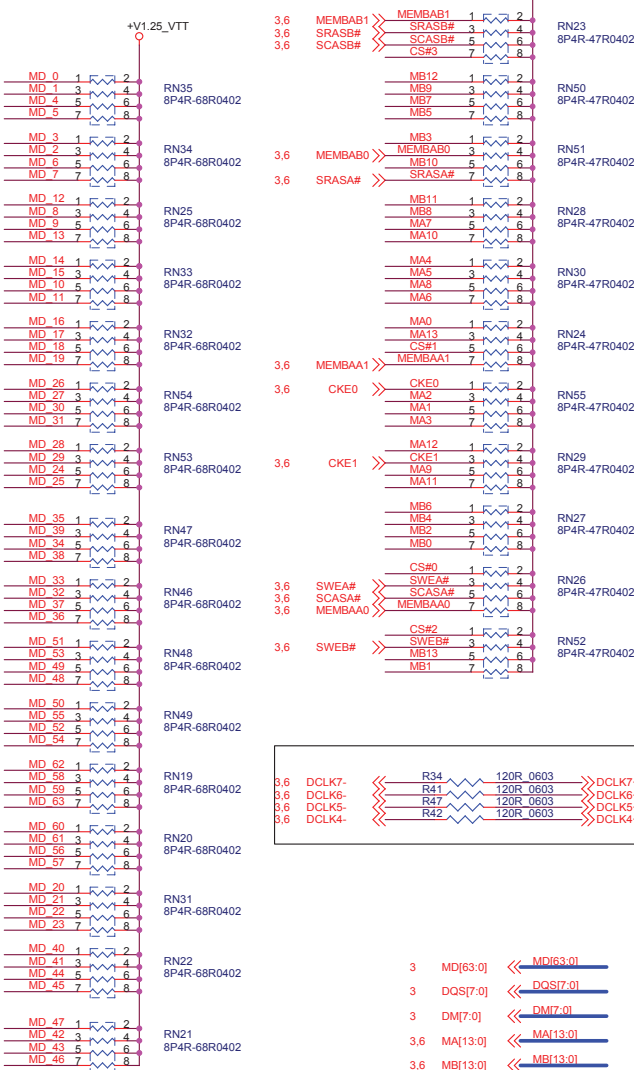
Place these two decoupling caps near DIMMs



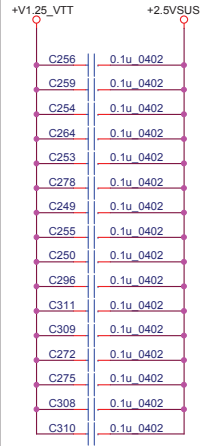
From CPU To DDR Socket



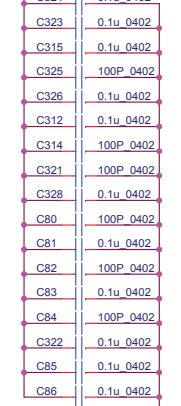
To DDR Socket



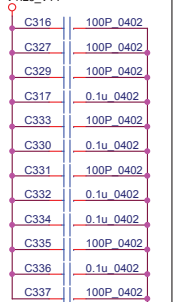
For EMI



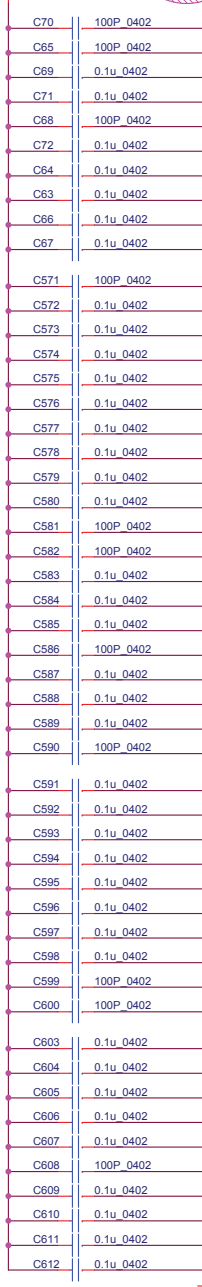
+V1.25_VTT



+V1.25_VTT



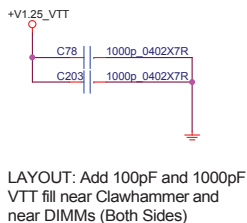
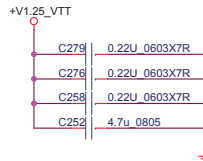
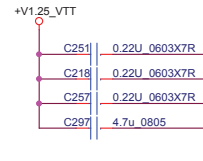
+2.5VSUS



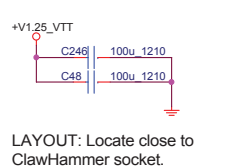
LAYOUT: Place alternating caps to GND and +2.5VDIMM in a single line along VTT island.

FOR EMI CLOSE RN7,13,47,19,25,28,37,39,41,45

LAYOUT: Place a cap every 1 inch on VTT trace between Clawhammer and DDR.



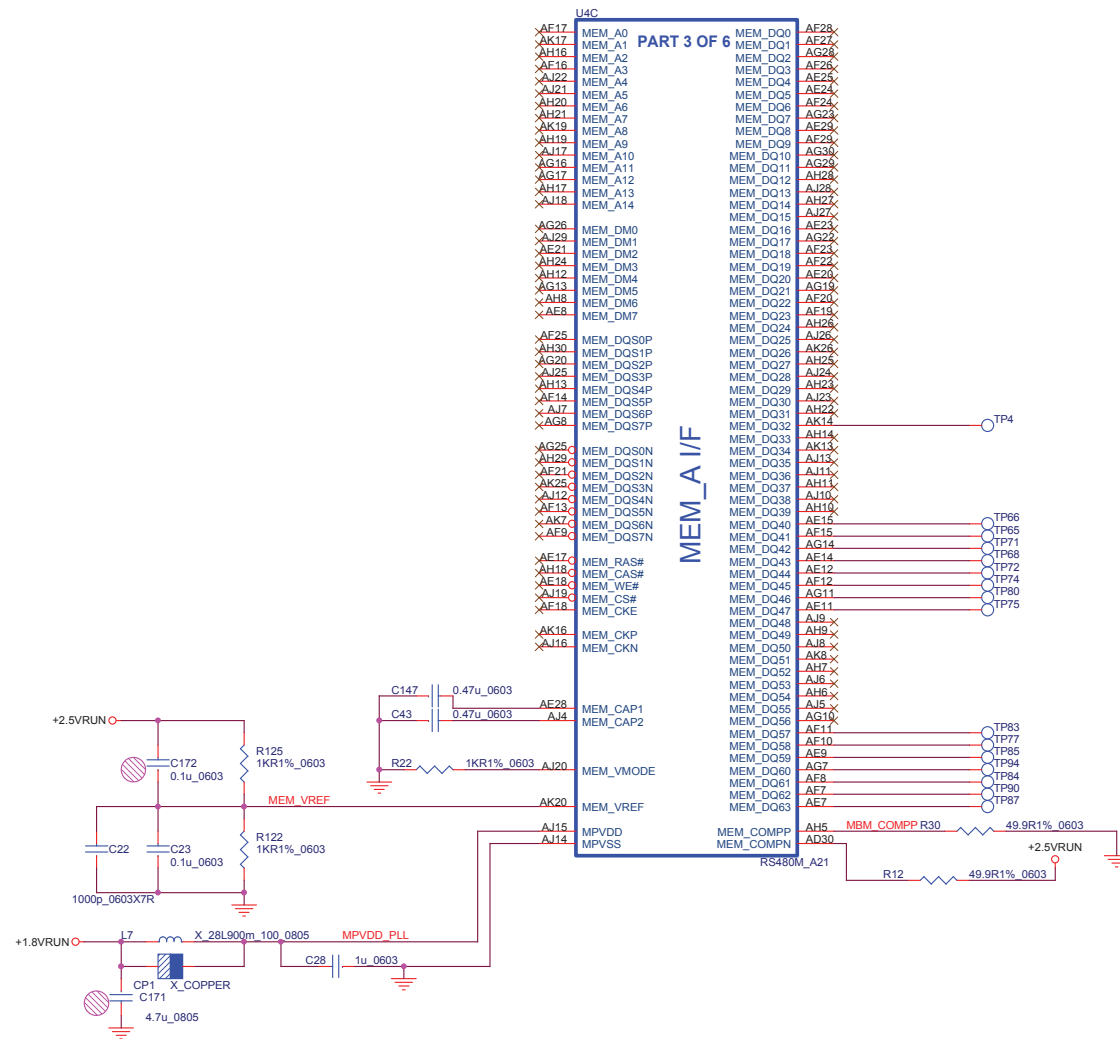
LAYOUT: Add 100pF and 1000pF VTT fill near Clawhammer and near DIMMs (Both Sides)

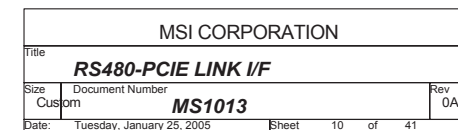


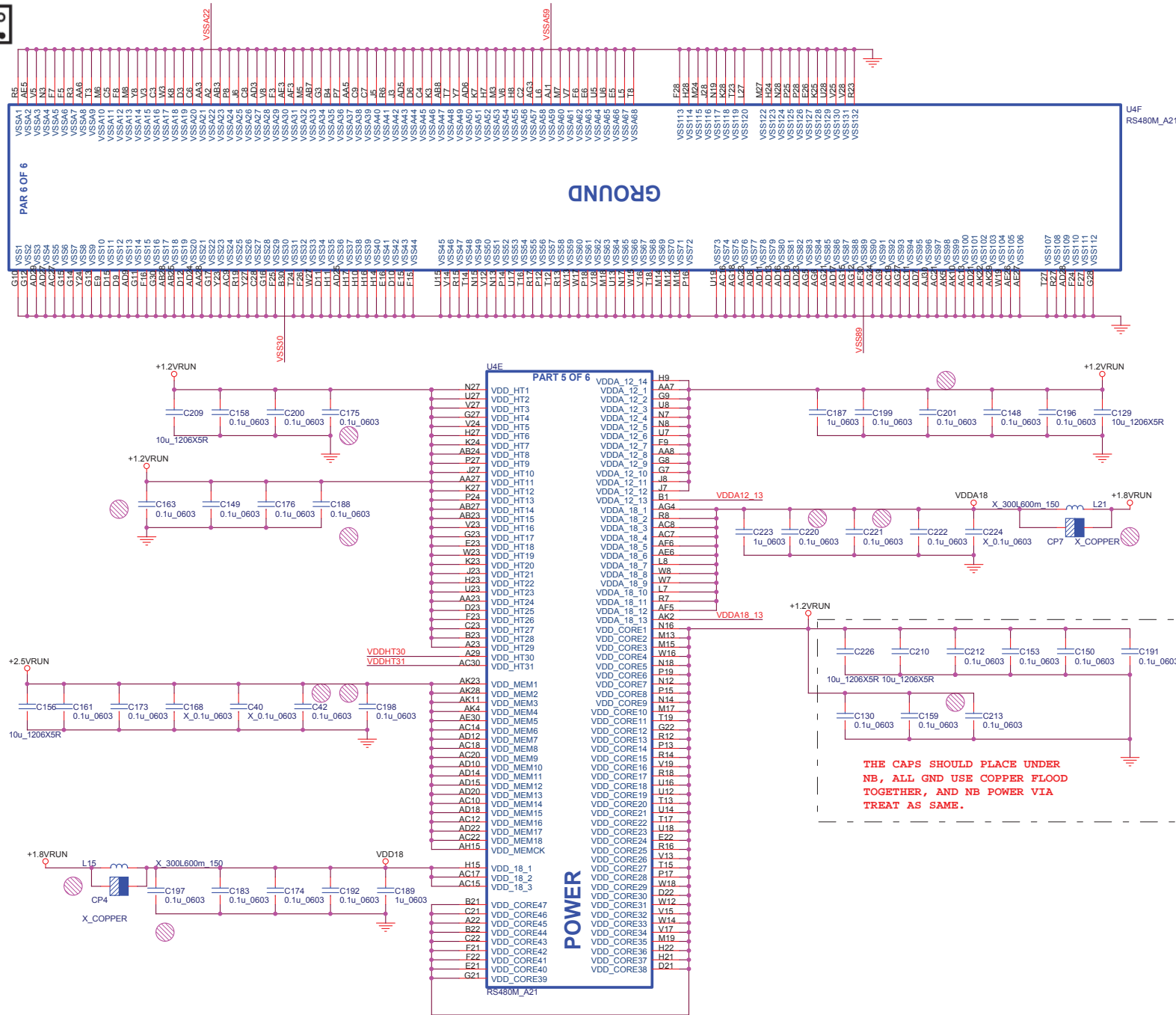
LAYOUT: Locate close to ClawHammer socket.

MSI CORPORATION

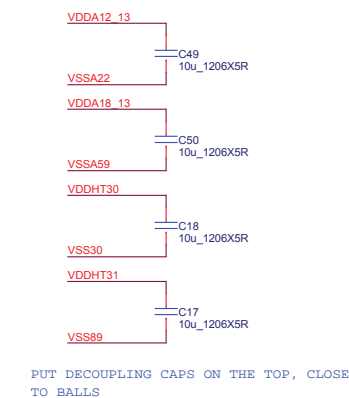
Title			DDR TERMINATION
Size	Document Number	Rev	0A
Custom	MS1013		
Date:	Tuesday, January 25, 2005	Sheet	7 of 41



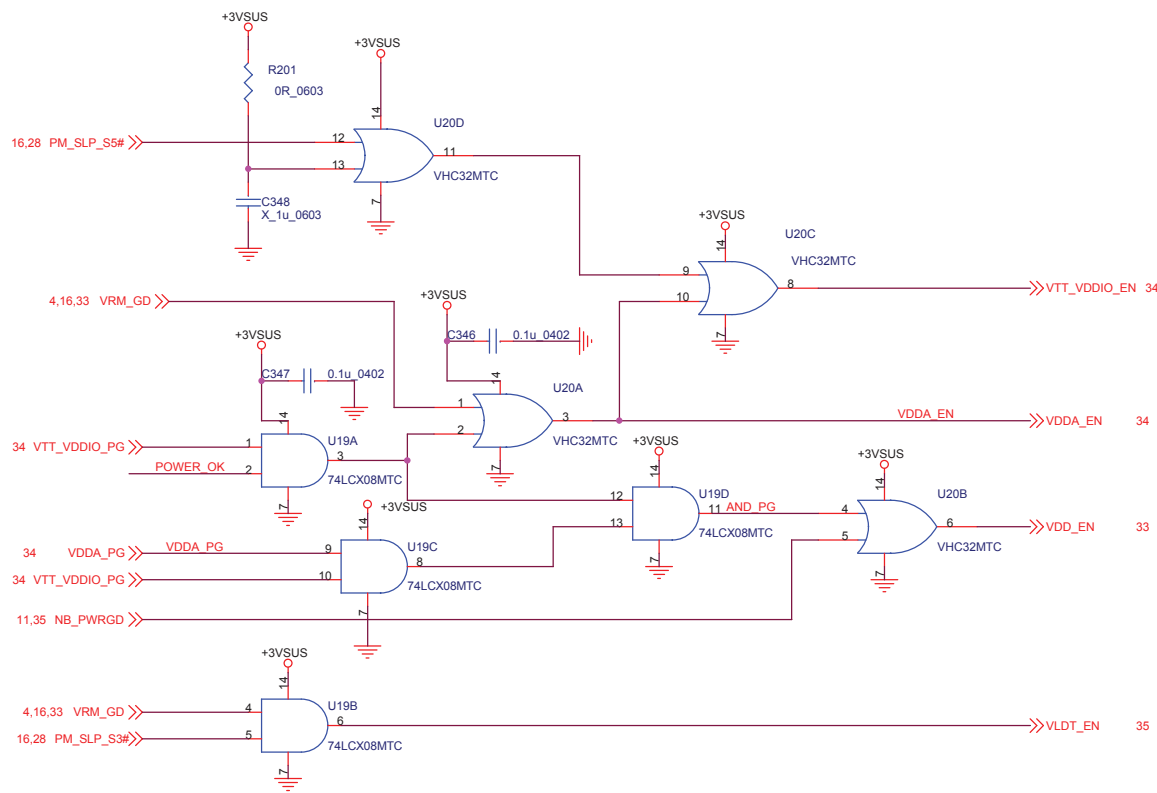




NB RS480 POWER STATES					
Power	Signal	S0	S1	S3	S4/S5
VDDHT		ON	ON	OFF	OFF
VDDR, VDDRCK		ON	ON	OFF	OFF
VDD18		ON	ON	OFF	OFF
VDDC		ON	ON	OFF	OFF
VDDA18		ON	ON	OFF	OFF
VDDA12		ON	ON	OFF	OFF
AVDD		ON	ON	OFF	OFF
AVDDDI		ON	ON	OFF	OFF
PLLVDD		ON	ON	OFF	OFF
HTPVDD		ON	ON	OFF	OFF
VDDR3		ON	ON	OFF	OFF
LPVDD		ON	ON	OFF	OFF
LVDDR18		ON	ON	OFF	OFF
LVDDR25		ON	ON	OFF	OFF

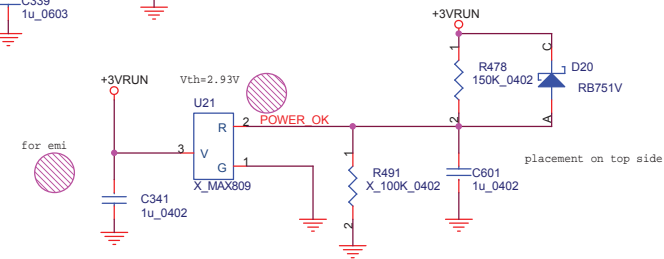
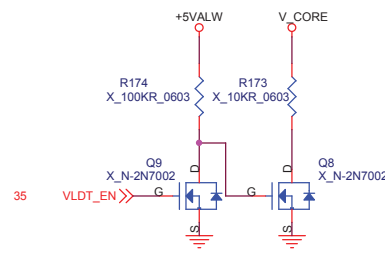
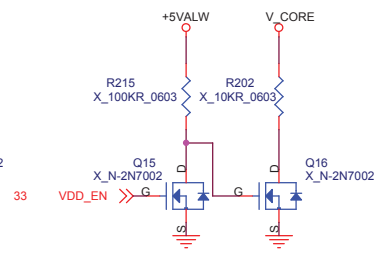
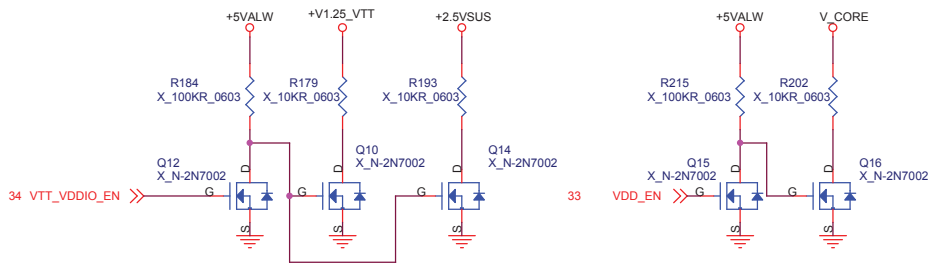
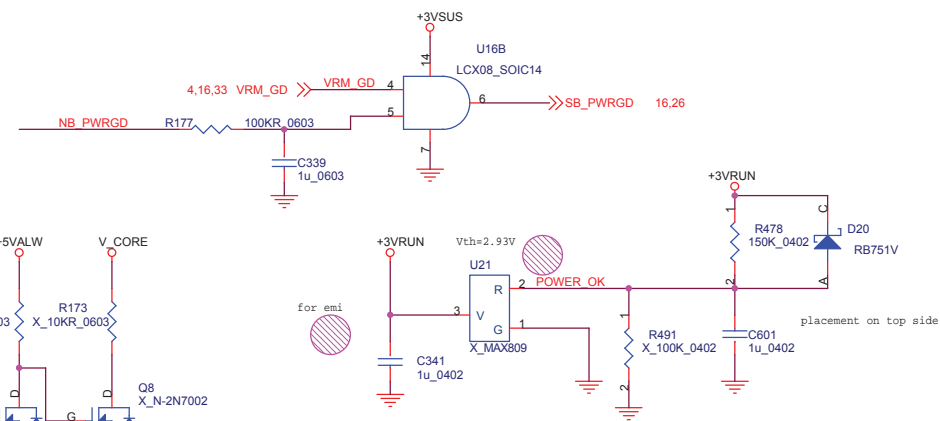


PUT DECOUPLING CAPS ON THE TOP, CLOSE TO BALLS

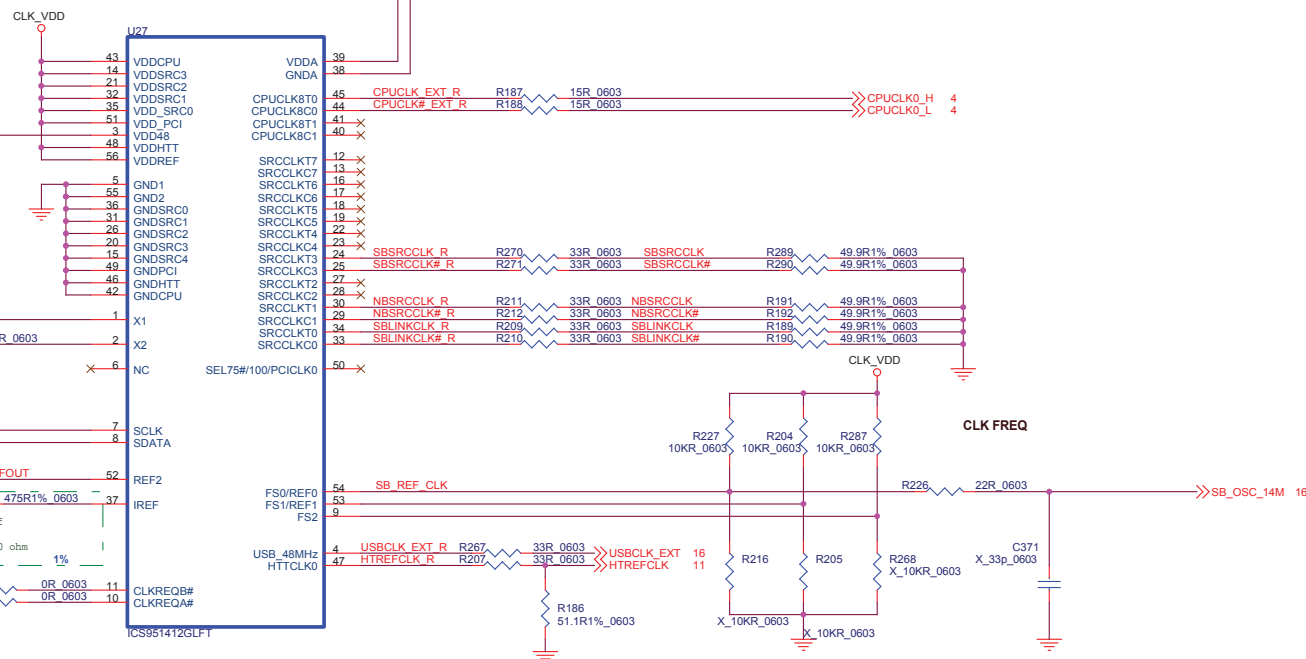
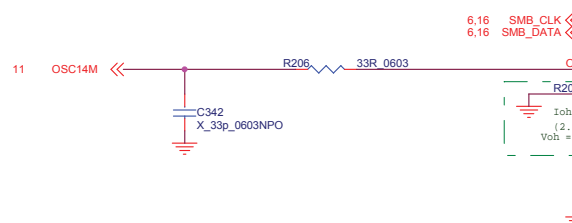
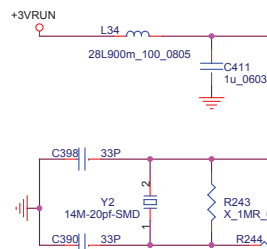
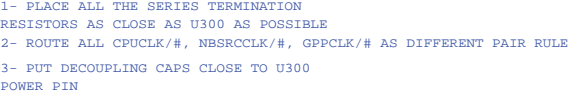
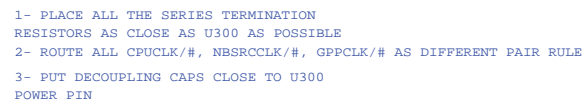


VHC32MTC-VCC=3.0
 VIH=0.7VCC
 VIL=0.3VCC
 VOH=2.9V
 VOL=0.1V

74LCX08MTC-VCC=3.0V
 VIH=2.0V
 VIL=0.8V
 VOH=2.4V
 VOL=0.4V



Title		(Title)
Size	Document Number	
A3	(Doc)	
Date:	Tuesday, January 25, 2005	Sheet 13 of 41
Rev		(RevCode)



OVERLAP COMMON PADS FOR DUAL-OP
RESISTORS

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

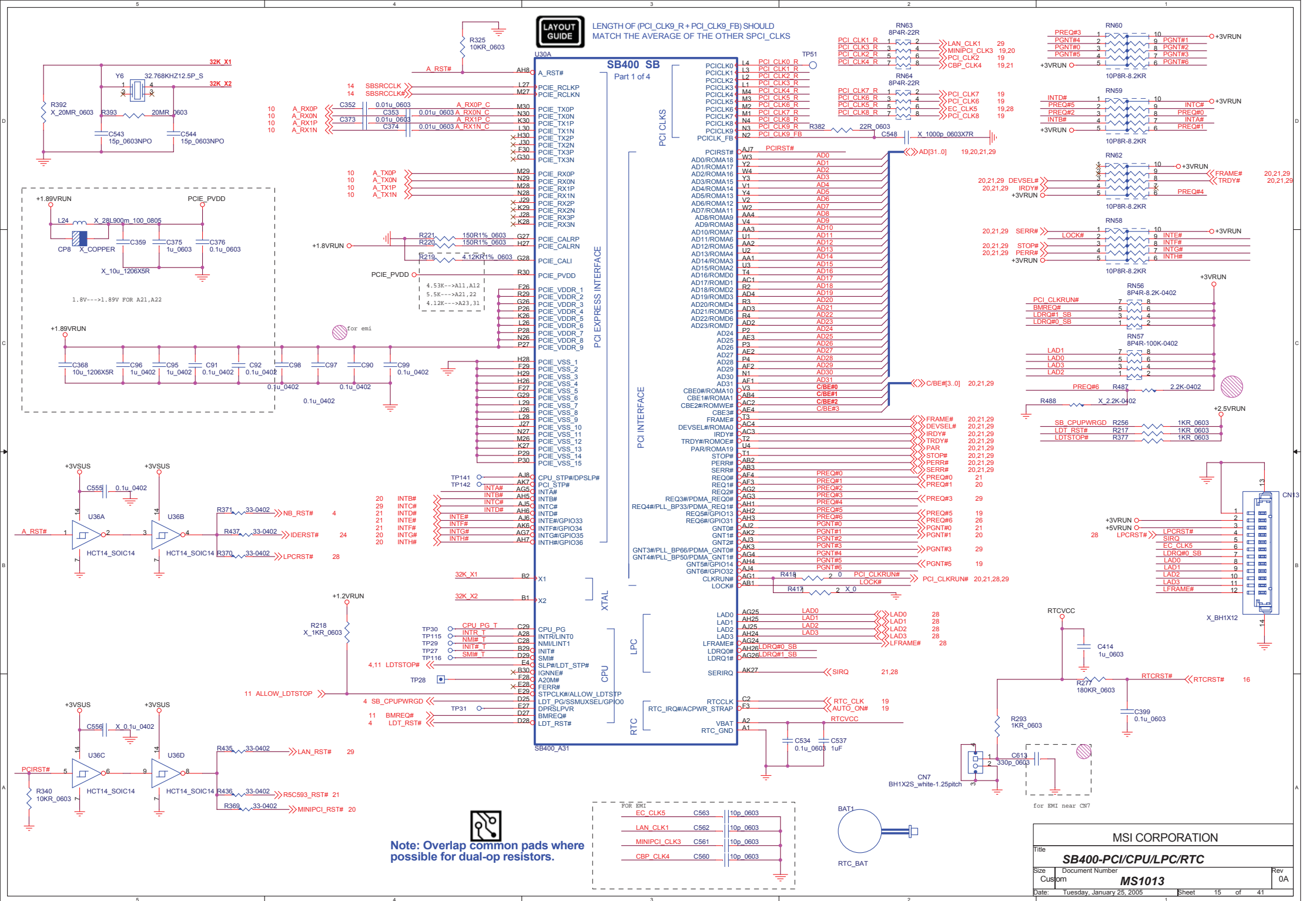


FOR



LAYOUT GUIDE

LENGTH OF (PCI_CLK9_R + PCI_CLK9_FB) SHOULD MATCH THE AVERAGE OF THE OTHER SPCL_CLKS



NOTE: ONLY USE FUNDAMENTAL MODE CRYSTAL

SB_PWRGD IS 50ms
AFTER NB_PWRGD

R144 CLOSE TO AC97

200mA
rating

MSI CORPORATION

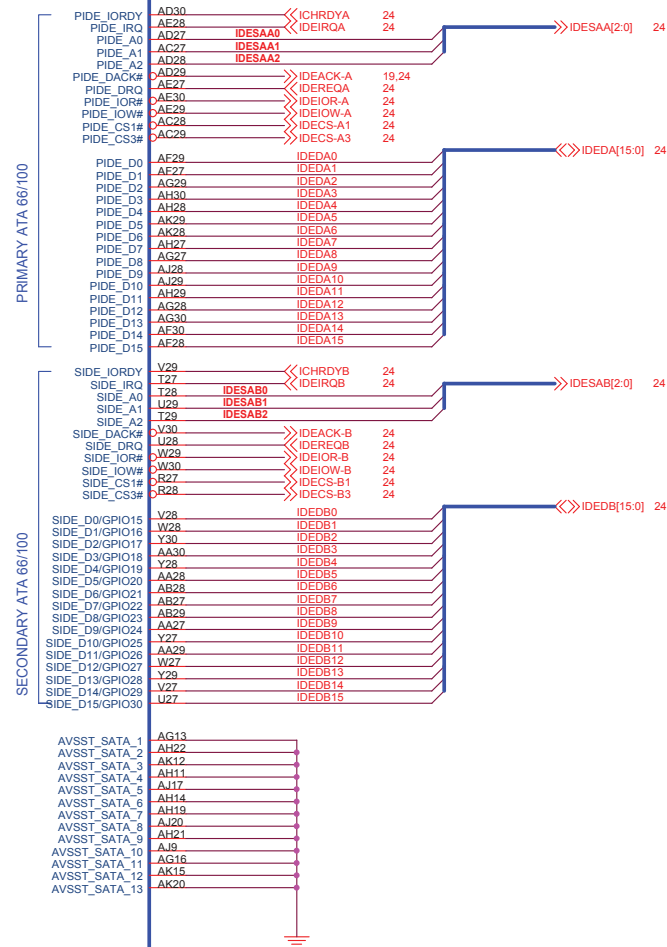
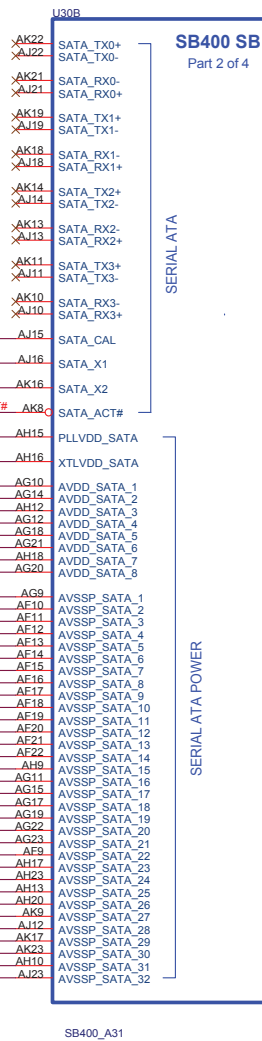
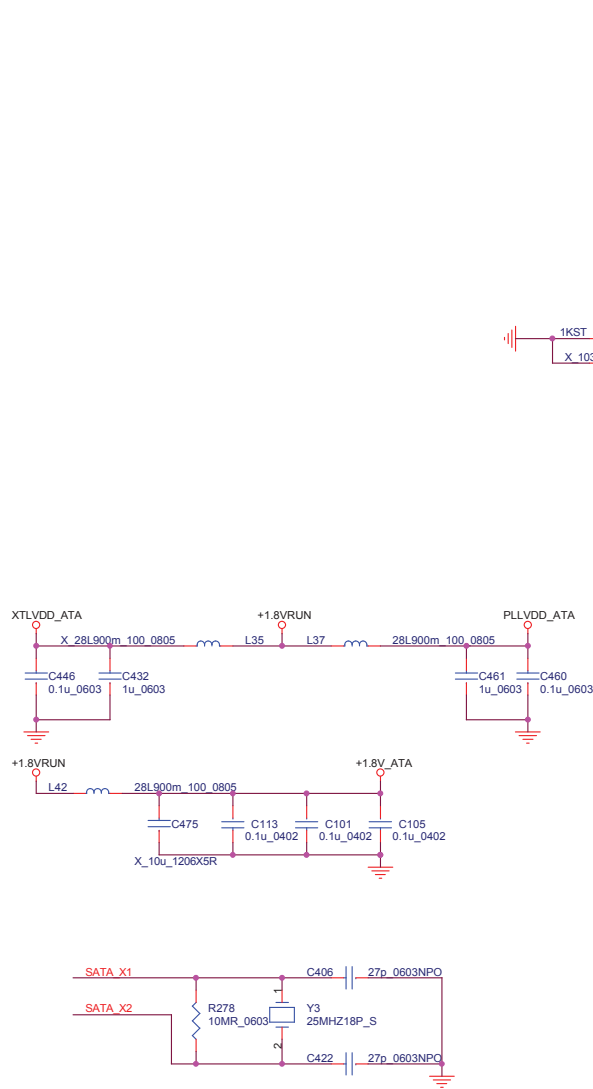
Title
SB400-ACPI/GPIO/AC97/USB

Size
Custom

Document Number
MS1013

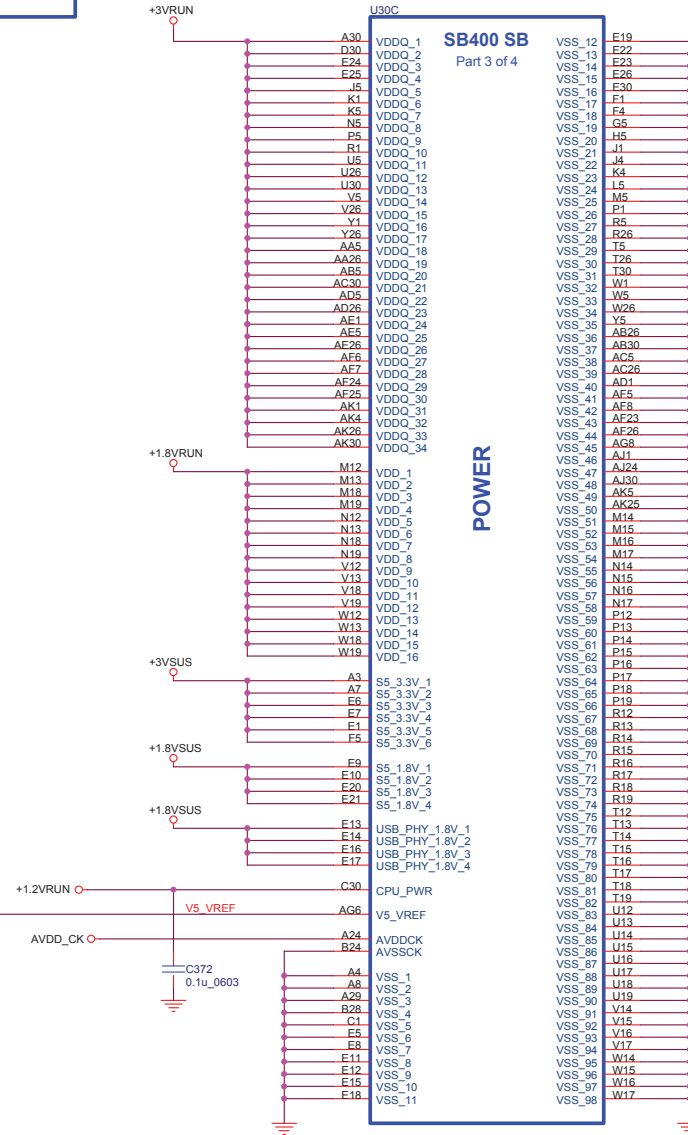
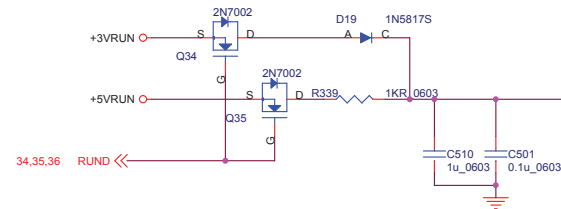
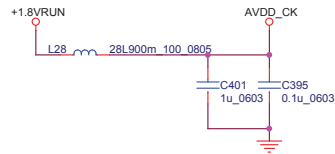
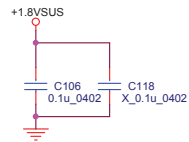
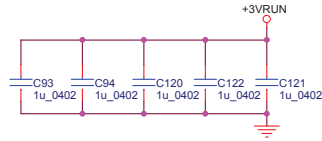
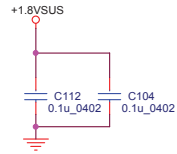
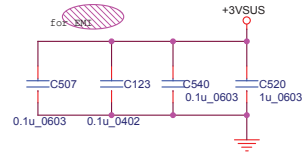
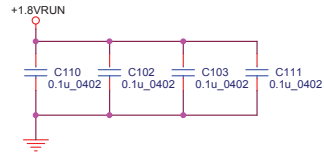
Rev
0A

Date: Tuesday, January 25, 2005 Sheet 16 of 41



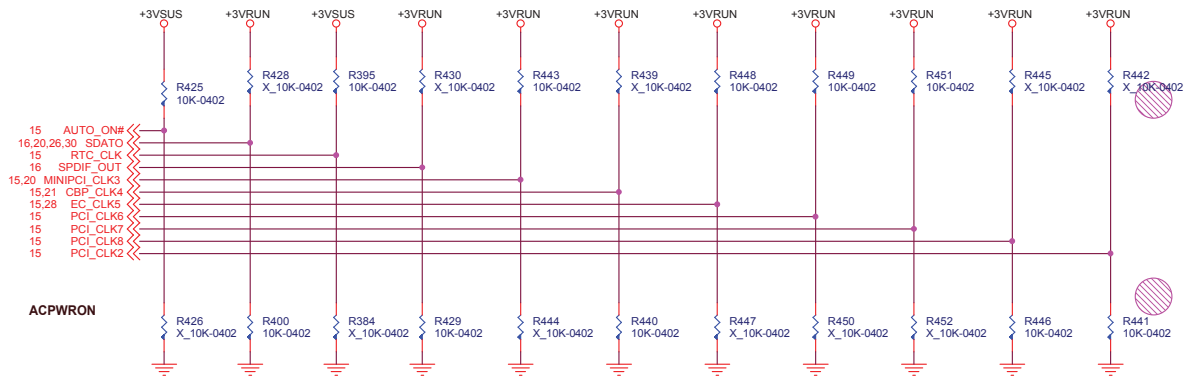


Place all the decoupling caps
on this sheet close to SB.



SB400_A31

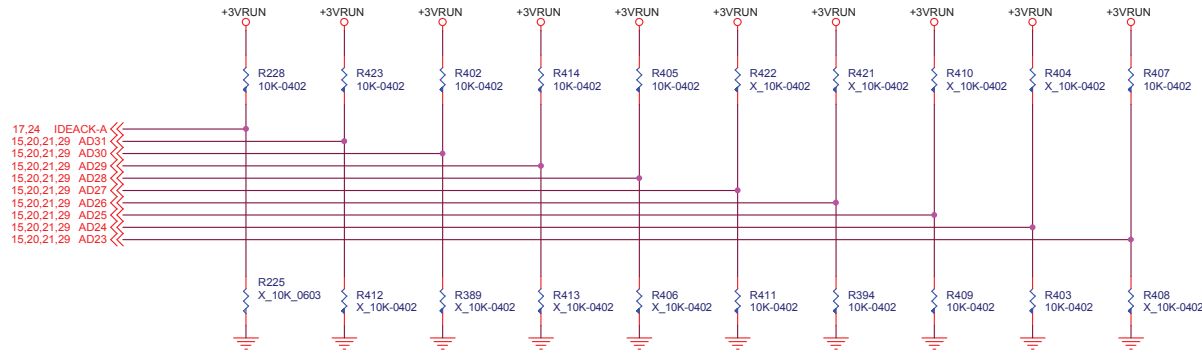
MSI CORPORATION			
Title			
SB400-PWR & DECOUPLING			
Size	Document Number	Rev	
Custom	MS1013	0A	
Date:	Tuesday, January 25, 2005	Sheet	18 of 41



STRAP FOR SB-A21

Note: Overlap common pads where possible for dual-op resistors.

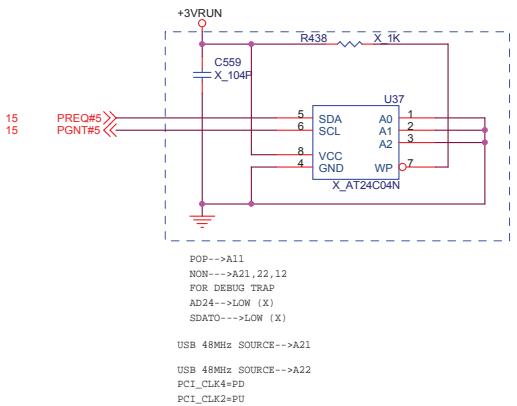
	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7	PCI_CLK8	PCI_CLK2
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	USB PHY PWRDOWN DISABLE DEFAULT	INTERNAL 48MHz PLL	14MHz OSC MODE from clock gen DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM I DEFAULT		48MHz OSC MODE DEFAULT
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	USB PHY PWRDOWN ENABLE	EXTERNAL 48MHz DEFAULT	14MHz XTAL MODE	CPU I/F = P4			48MHz XTAL MODE



	PDAK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	PLL CHARGE PUMP CTRL BIT 1 HI DEFAULT	PLL CHARGE PUMP CTRL BIT 0 HI DEFAULT	PLL VCO CTRL BIT 1 HI DEFAULT	PLL VCO CTRL BIT 0 HI DEFAULT	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	USE USB PLL DEFAULT
PULL LOW	USE SHORT RESET	PLL CHARGE PUMP CTRL BIT 1 LO	PLL CHARGE PUMP CTRL BIT 0 LO	PLL VCO CTRL BIT 1 LO	PLL VCO CTRL BIT 0 LO	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BYPASS USB PLL

LONG RESET -->A21

SB PCIE EEPROM STRAPS



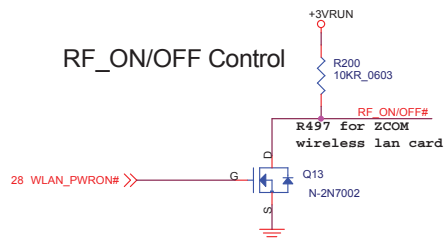
POP-->A11
NON-->A21,22,12
FOR DEBUG TRAP
AD24-->LOW (X)
SDATO-->LOW (X)

USB 48MHz SOURCE-->A21
USB 48MHz SOURCE-->A22
PCI_CLK4=PD
PCI_CLK2=PU

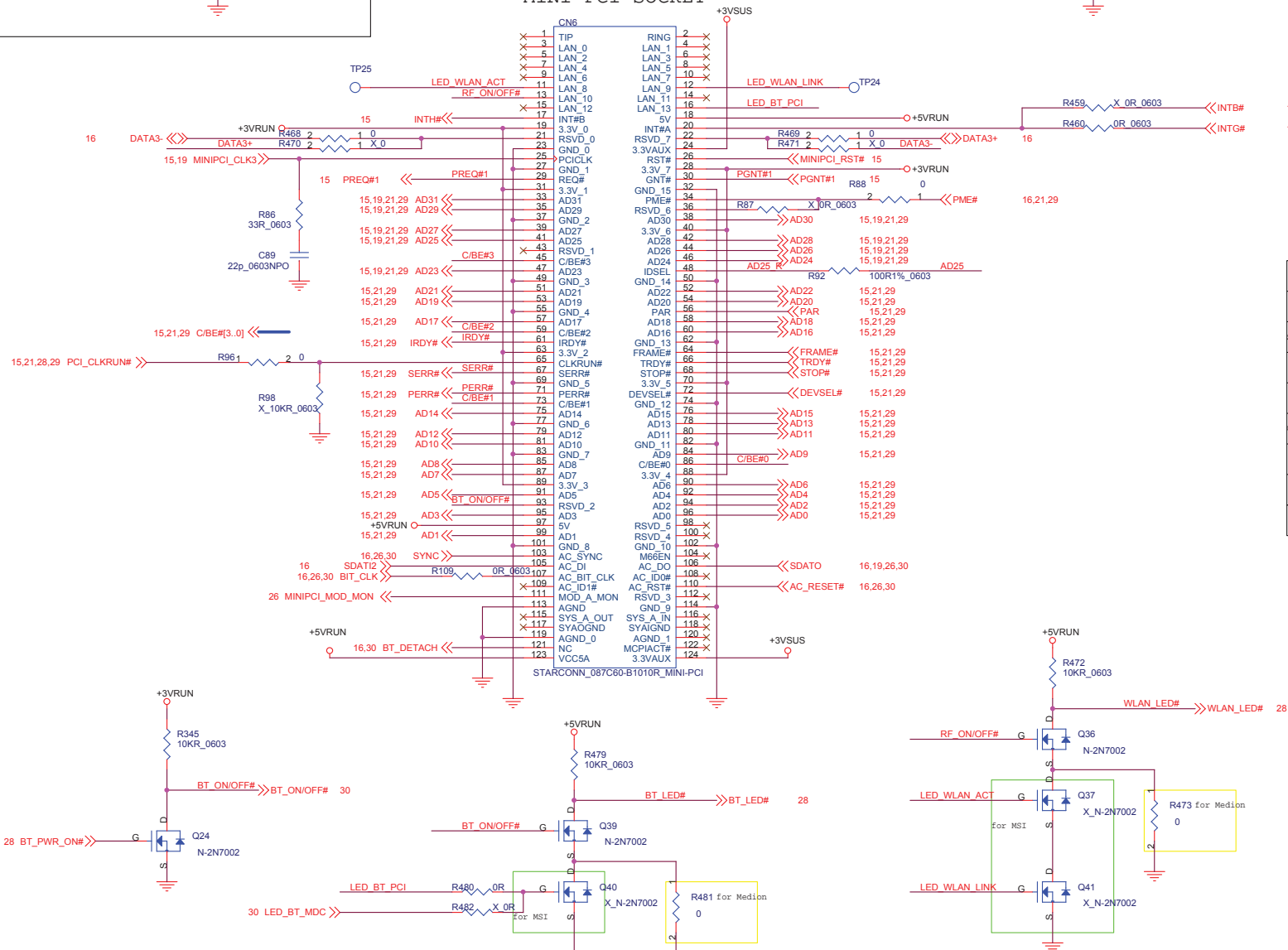
MSI CORPORATION

Title	SB400-STRAPS		
Size	Document Number	Rev	
Custom	MS1013	0A	
Date:	Tuesday, January 25, 2005	Sheet	19 of 41

RF_ON/OFF Control



MINI PCI SOCKET



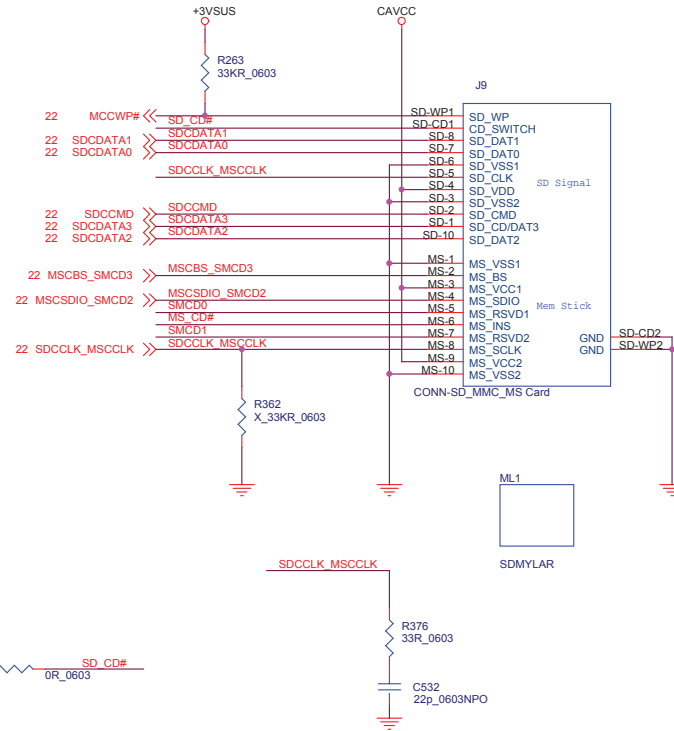
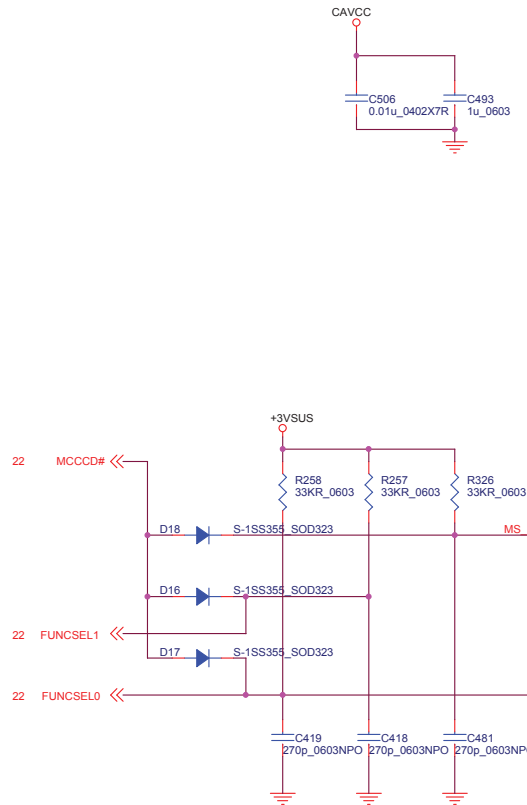
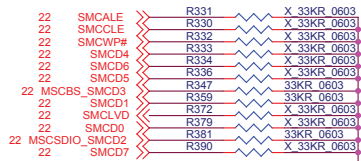
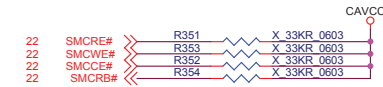
PCI RESOURCE

DEVICE	IDSEL#	REQ/GNT#	PCI_INT#	CLOCK
NB VGA	NA	NA	A	
SOUTHBRIDGE	AD31(INT)	NA	NA	NA
MINIPCI	AD25	1	G/H	PCI_CLK3
LAN	AD19	3	C	PCI_CLK1
CARDREADER	AD20	0	D/E/F	PCI_CLK4
USB	AD30	NA	D	INTERNAL
AC97	AD31	NA	B	INTERNAL
ATA100	AD31	NA	A	INTERNAL

AD[16:29] FOR DEVICE
AD[30:31] FOR SB INTERNAL DEVICE

MSI CORPORATION

Title	Mini-PCI Slot		
Size	Document Number	Rev	
Custom	MS1013	0A	
Date:	Tuesday, January 25, 2005	Sheet	20 of 41

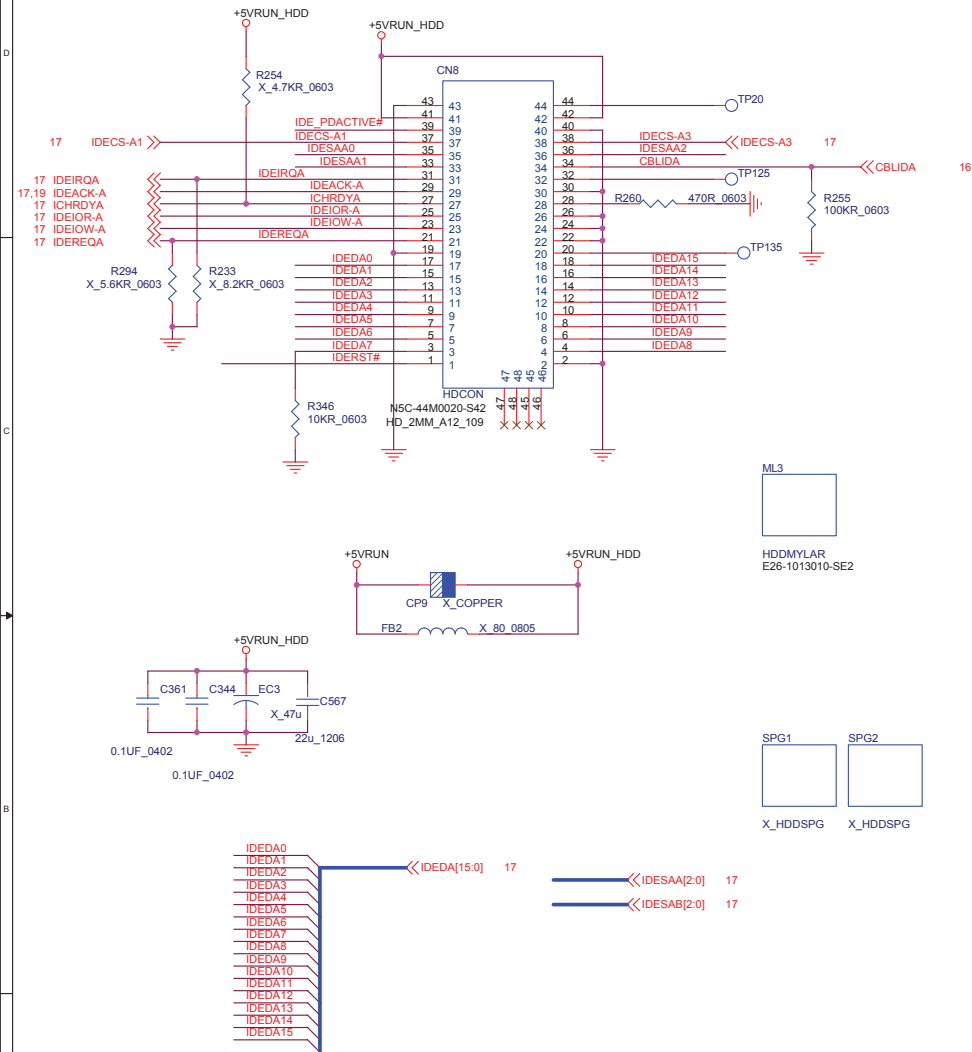


Memory Card Detect Logic Table

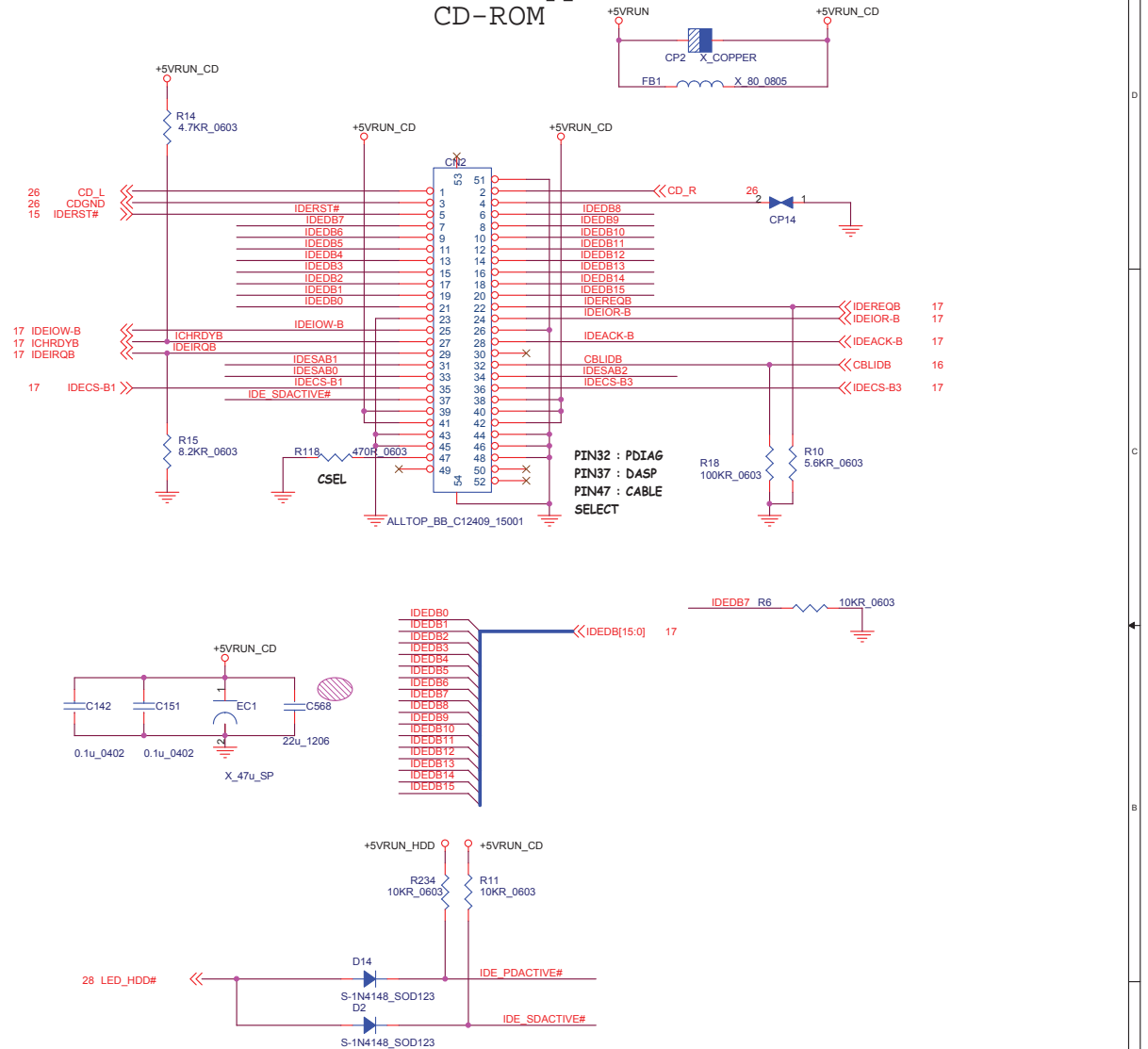
MS_CD#	SM_CD#	SD_CD#	->	Detected Card
0	0	0	->	INHIBIT
0	0	1	->	INHIBIT
0	1	0	->	INHIBIT
0	1	1	->	MemoryStick Detected
1	0	0	->	INHIBIT
1	0	1	->	SmartMedia Detected
1	1	0	->	SD/MMC Detected
1	1	1	->	Not Detected

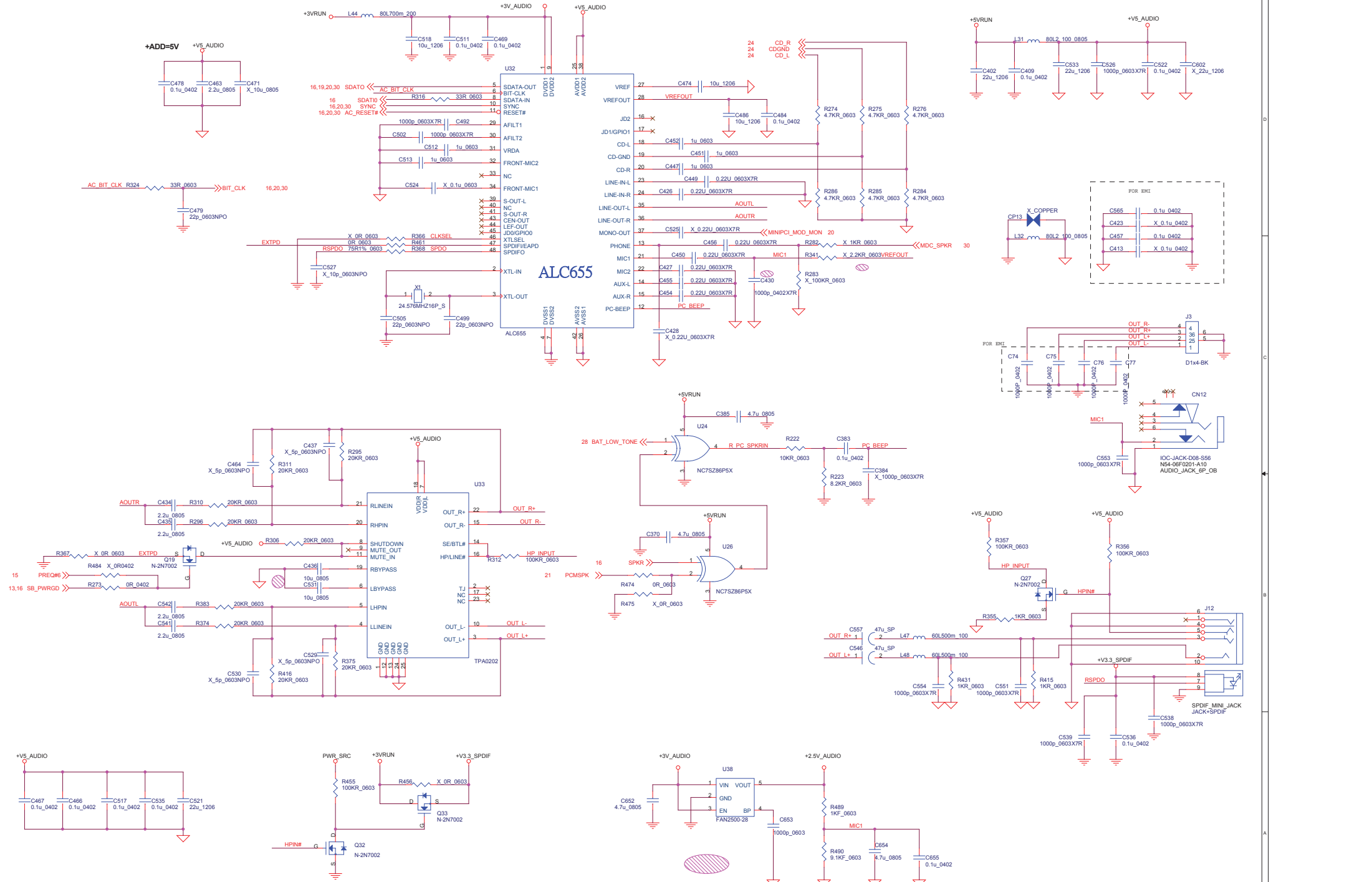
DO NOT INSERT SMARTMEDIA, SD/MMC AND MEMORYSTICK SIMULTANEOUSLY.

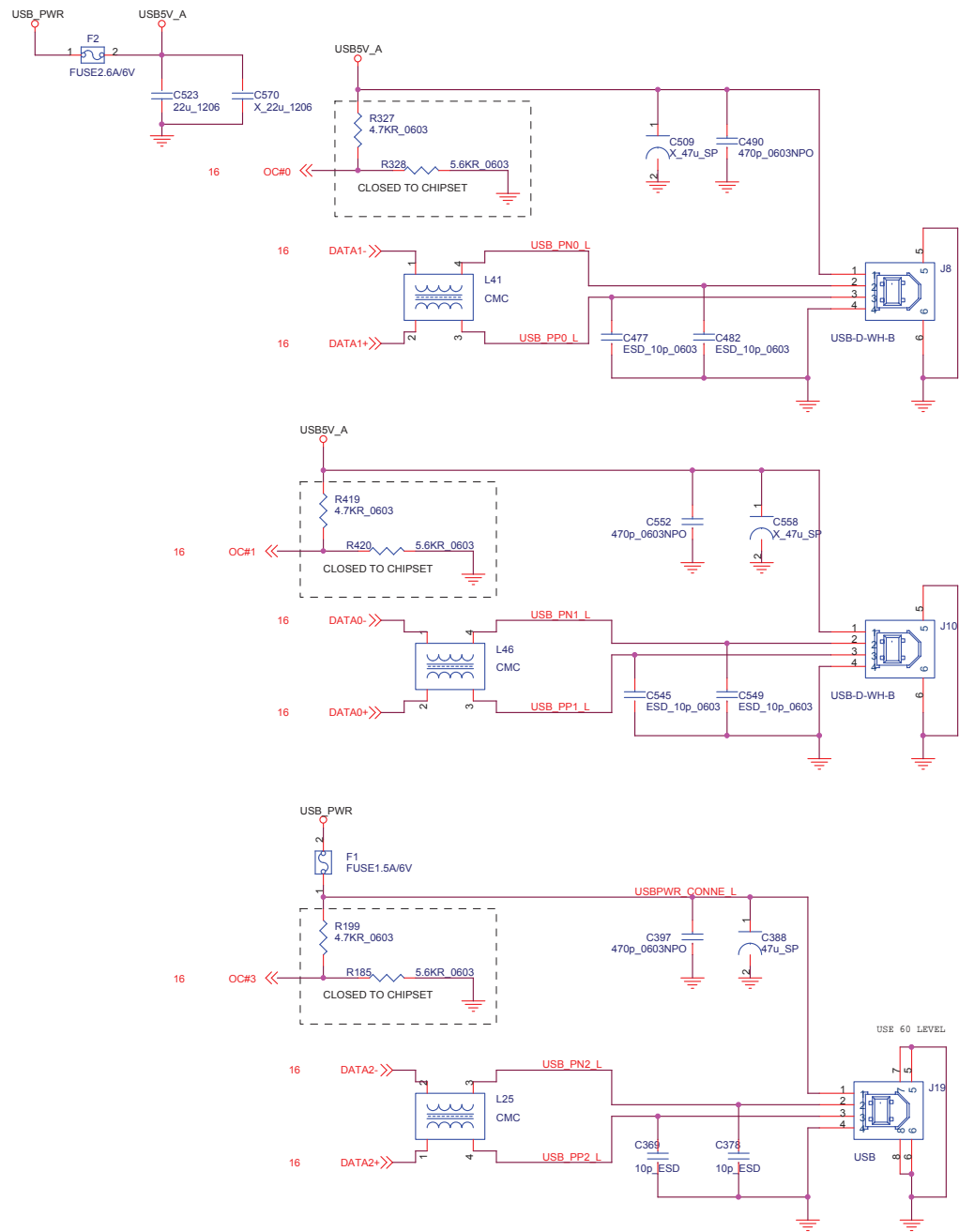
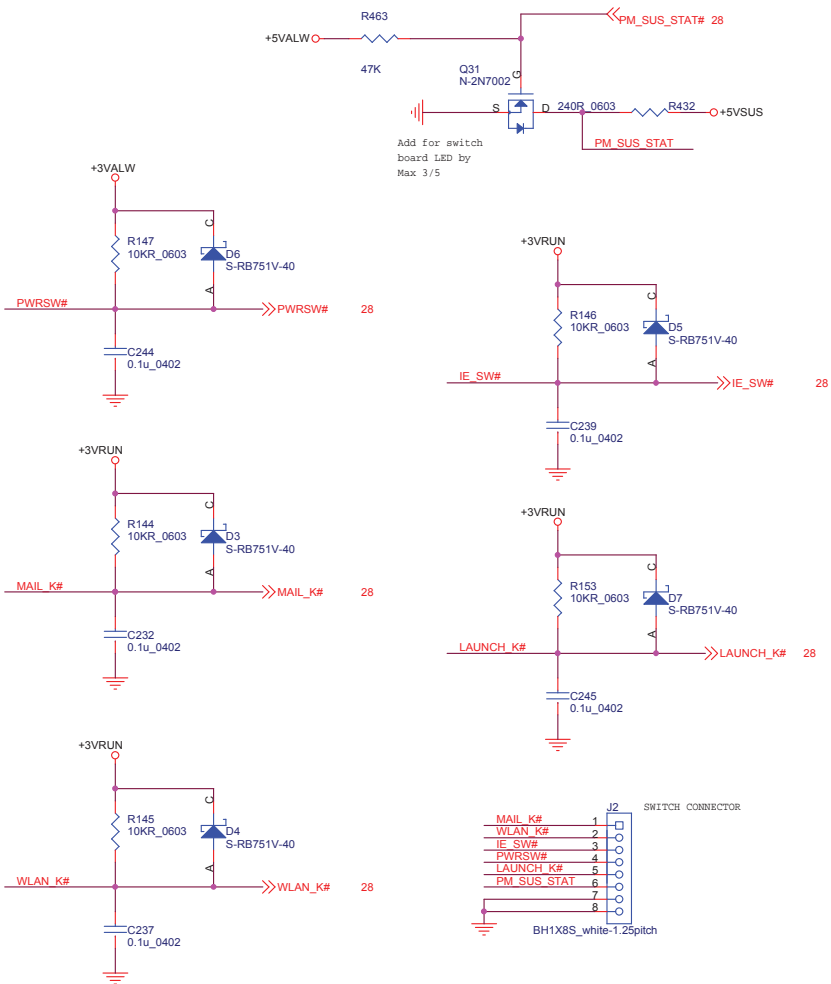
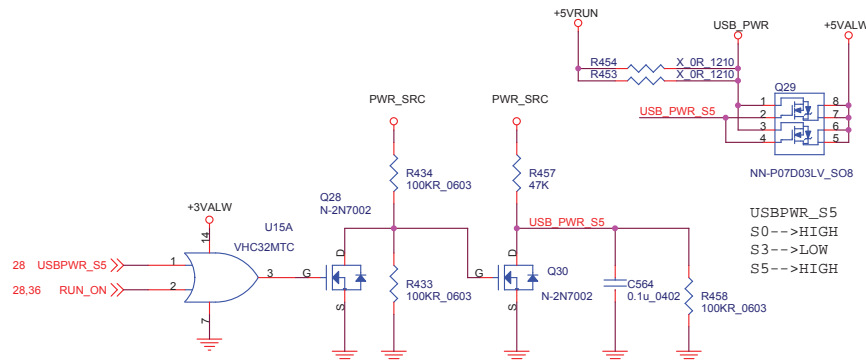
2.5"HD DRIVE



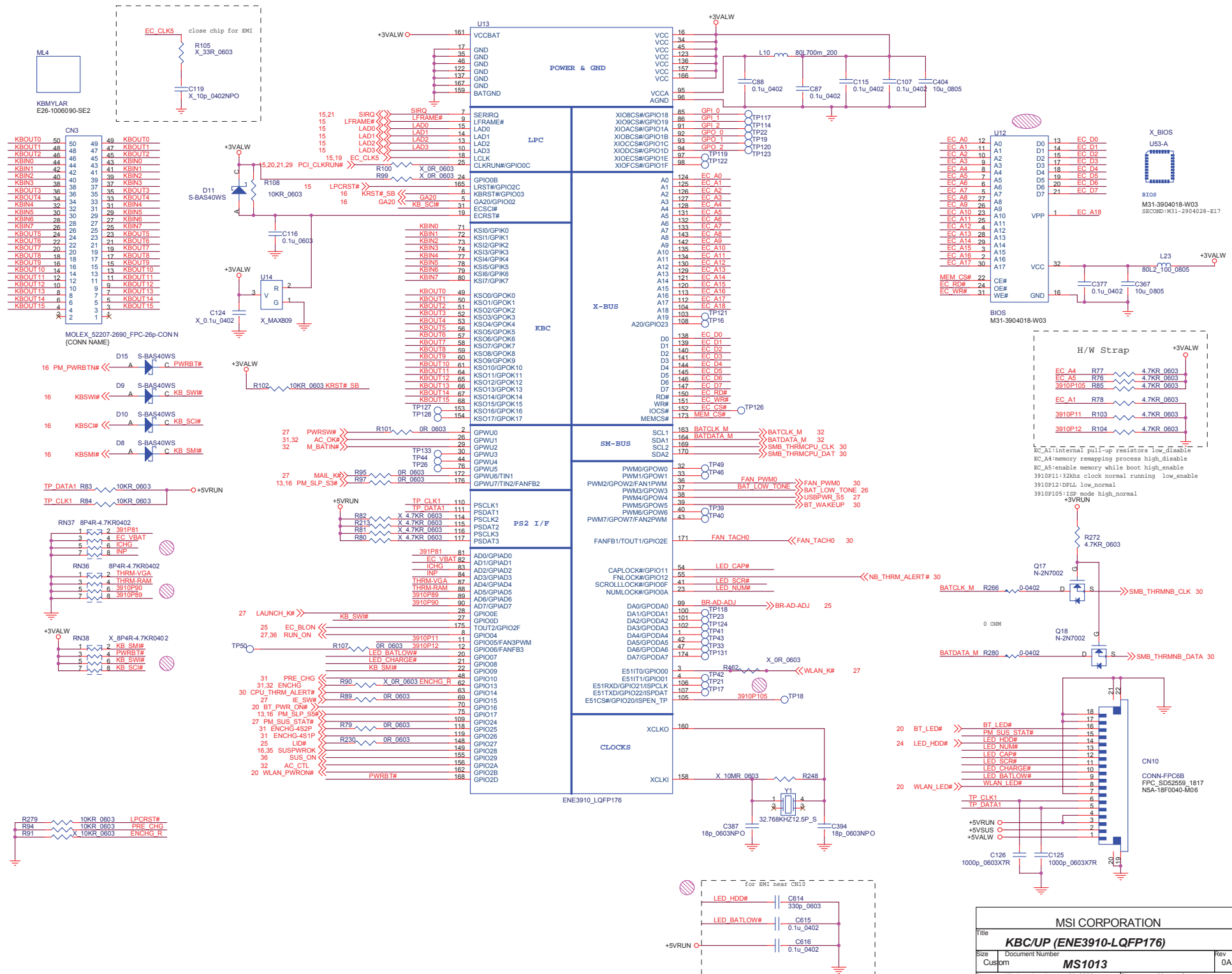
Slim Type CD-ROM

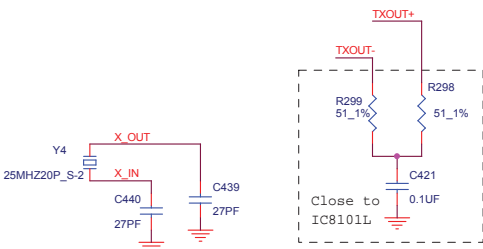






MSI CORPORATION		
Title	USB 2.0 CON x3 & LEDS & SW	
Size	Document Number	Rev
Custom	MS1013	0A
Date:	Tuesday, January 25, 2005	Sheet 27 of 41

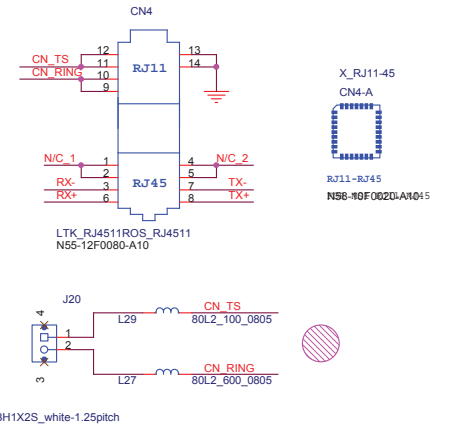
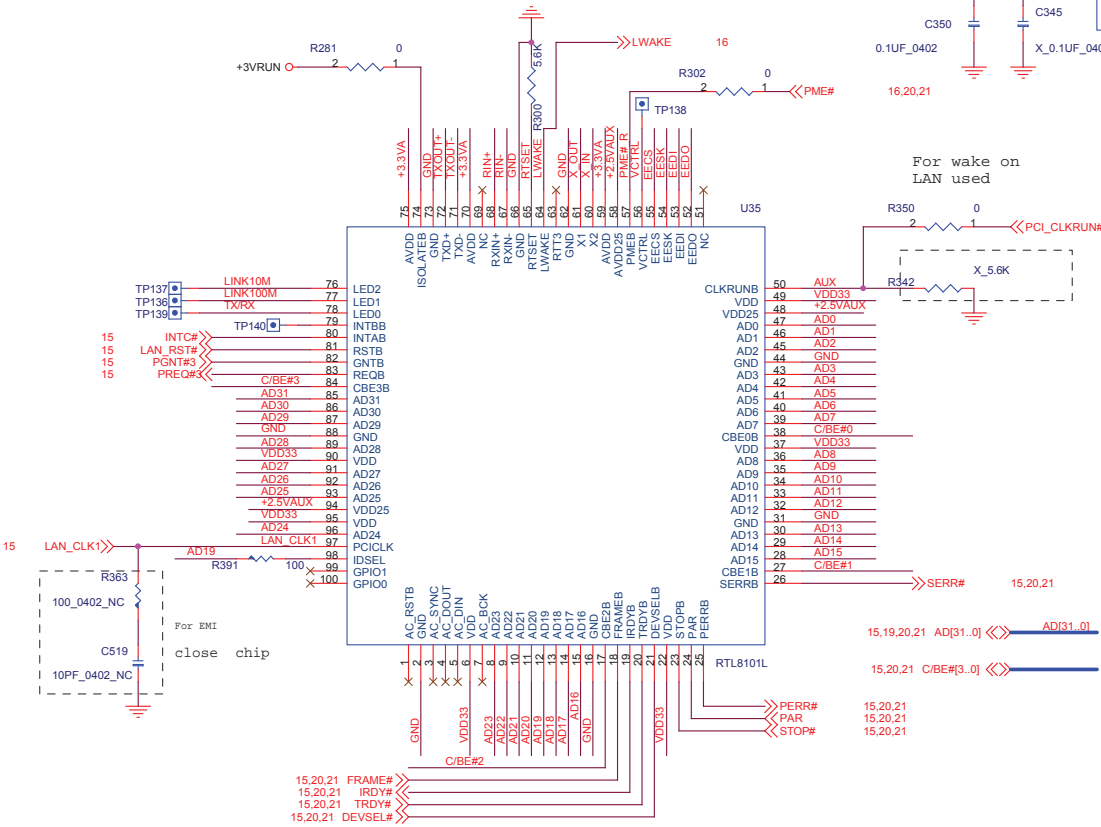
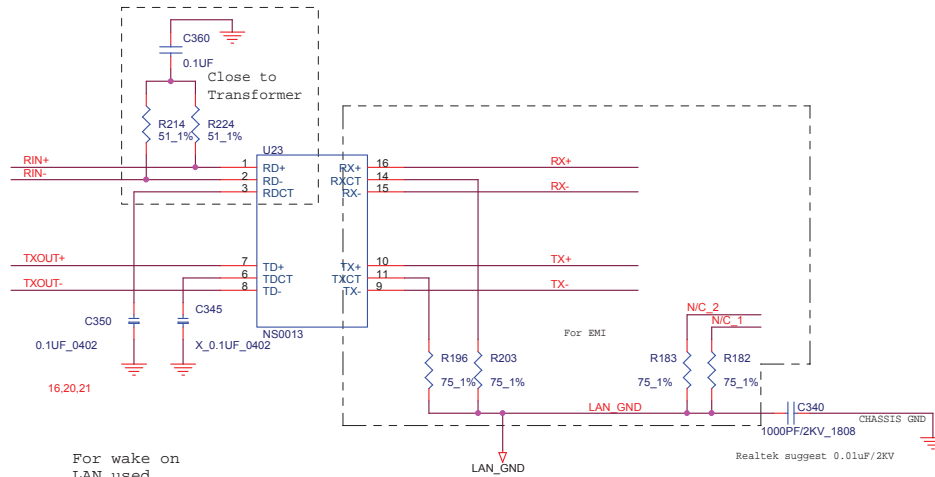




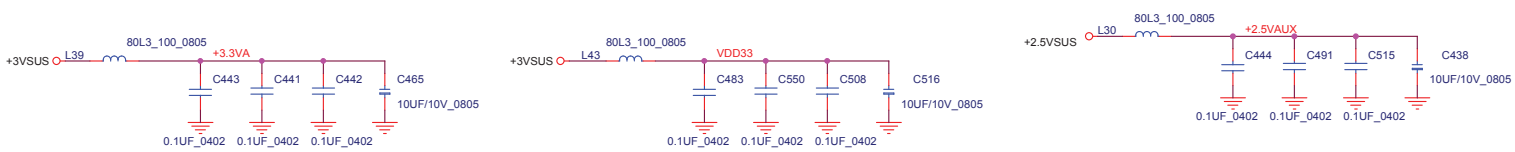
Lay out Rule :

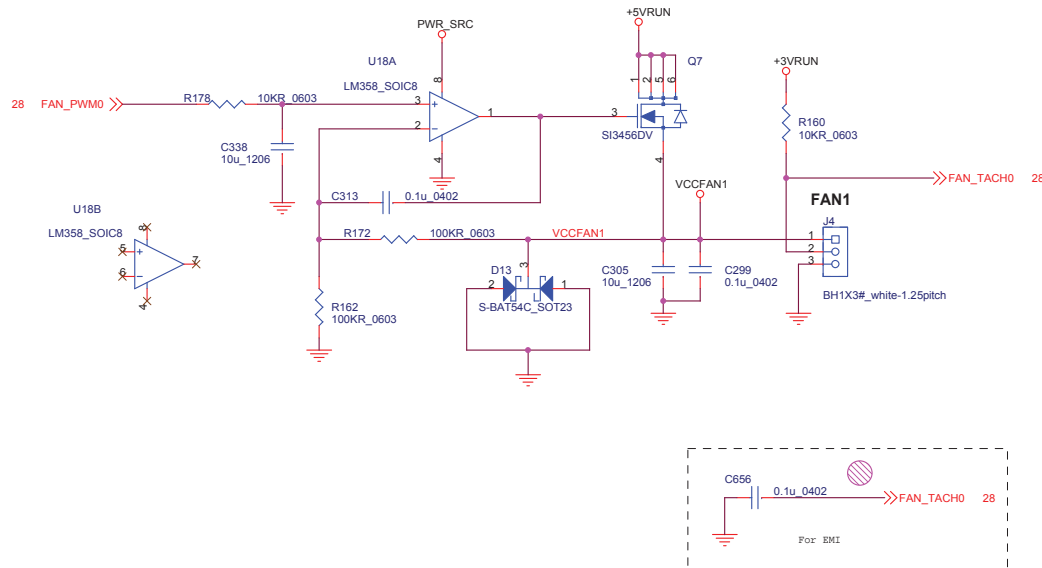
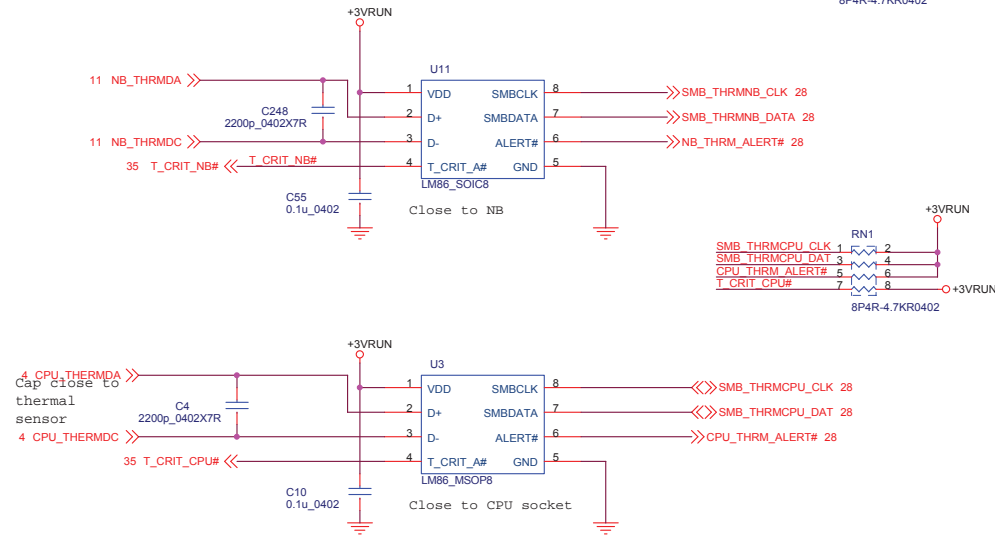
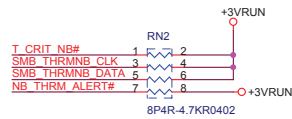
1. Tx+/- and Rx+/- length : +/-100mil
2. Through hole less .
3. Tx+/-
GND
Rx+/-

Ground separates Tx/Rx .

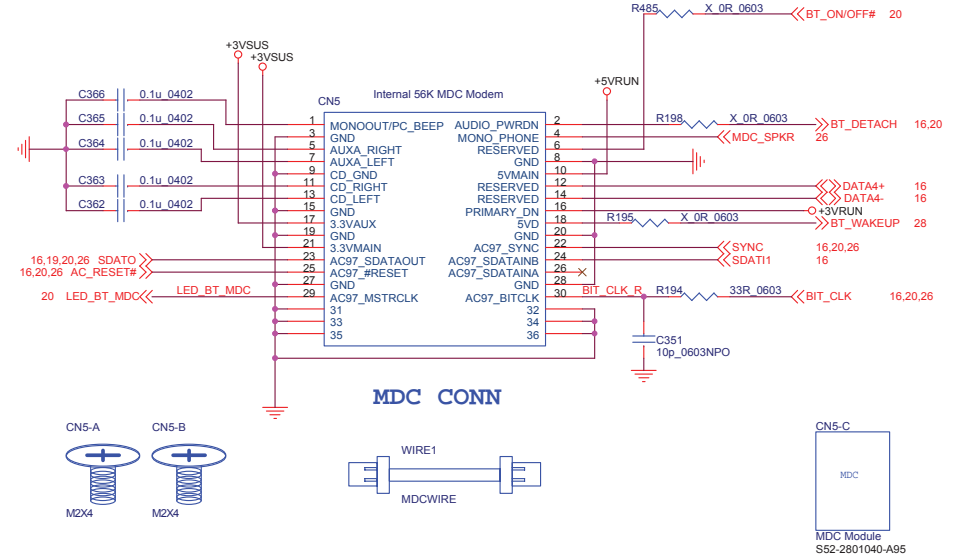


OTHER SIGNALS ARE FAR AWAY THIS TWO TRACES.
 *** THIS DISTANCE IS MIN. 2.5mm***
 ***THIS SPACE IS IN 3D SPACE AND INCLUDE ANY ***
 ***POWER ANG GROUND ***





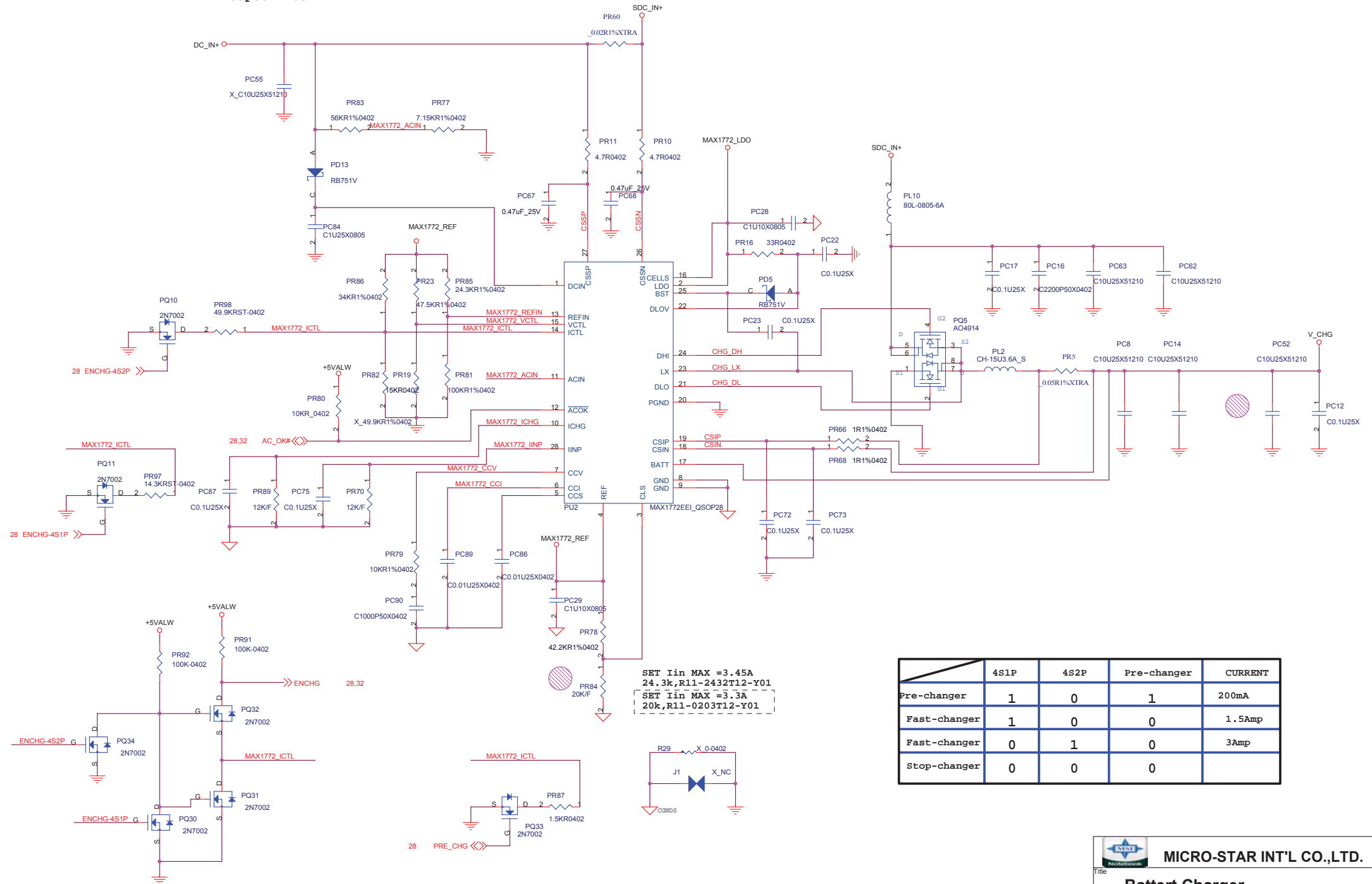
MDC



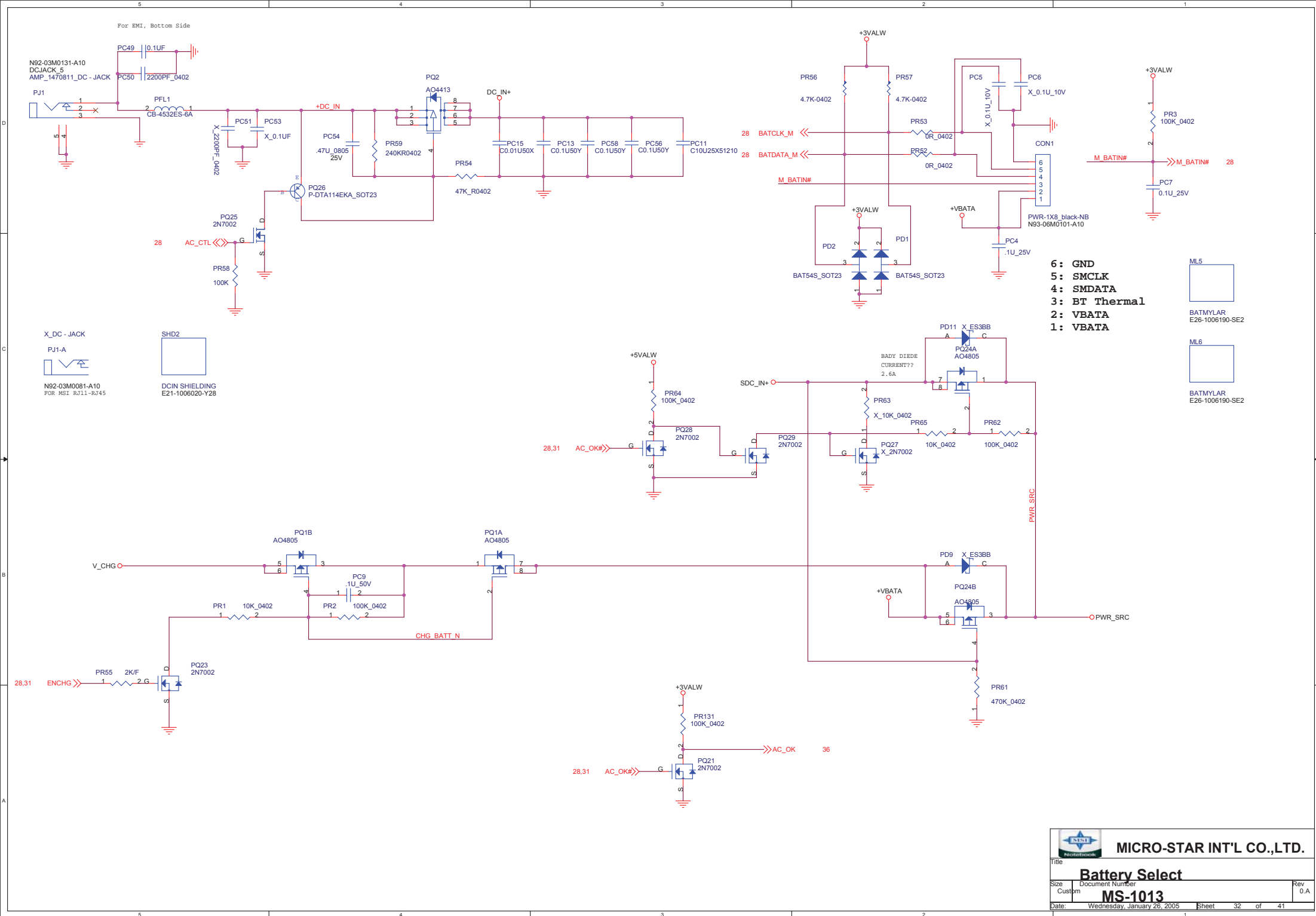
OTHER SIGNALS ARE FAR AWAY THIS TWO TRACES.
 *** THIS DISTANCE IS MIN. 2.5mm***
 ***THIS SPACE IS IN 3D SPACE AND INCLUDE ANY ***
 ***POWER ANG GROUND ***

MSI CORPORATION			
Title	HARDWARE MONITOR		
Size	Document Number	Rev	
Custom	MS1013	0A	
Date:	Tuesday, January 25, 2005	Sheet	30 of 41

Adapter= 65 W



	4S1P	4S2P	Pre-charger	CURRENT
Pre-charger	1	0	1	200mA
Fast-charger	1	0	0	1.5Amp
Fast-charger	0	1	0	3Amp
Stop-charger	0	0	0	



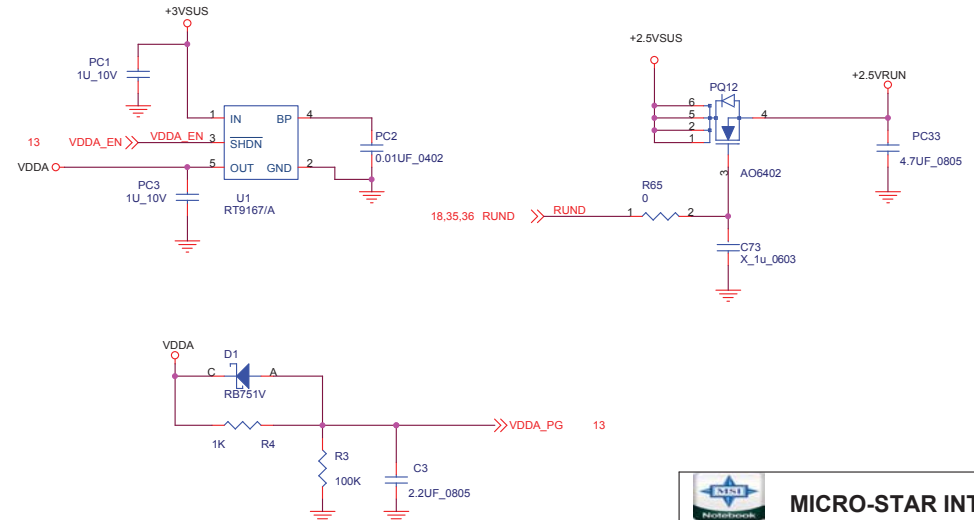
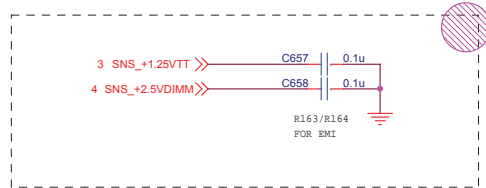
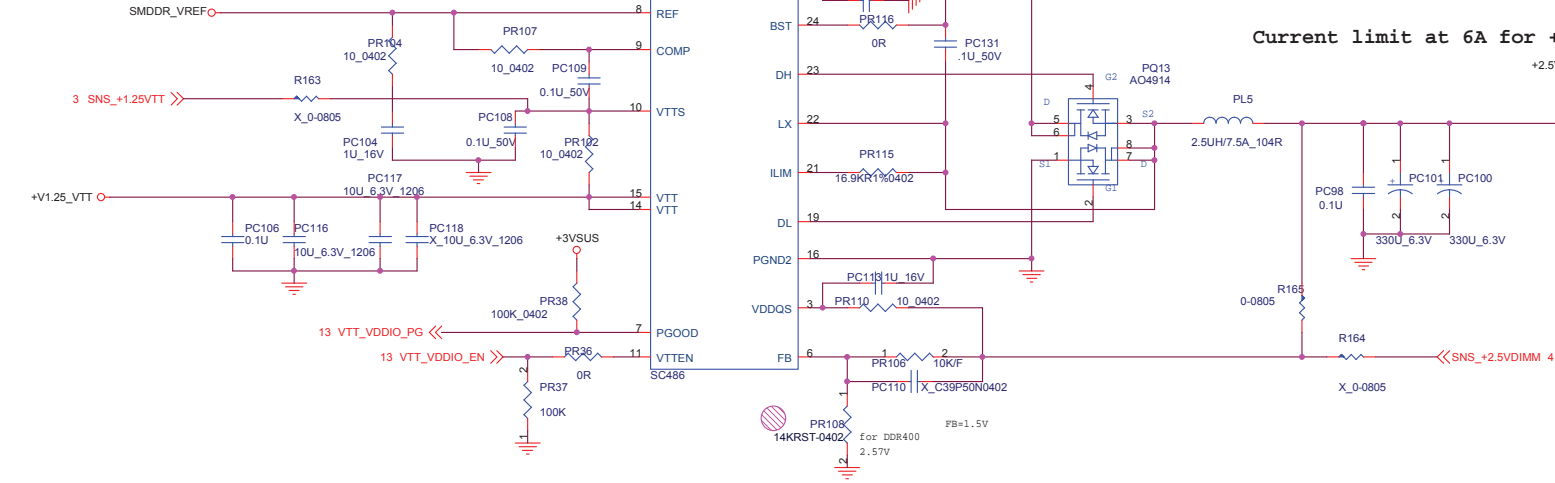


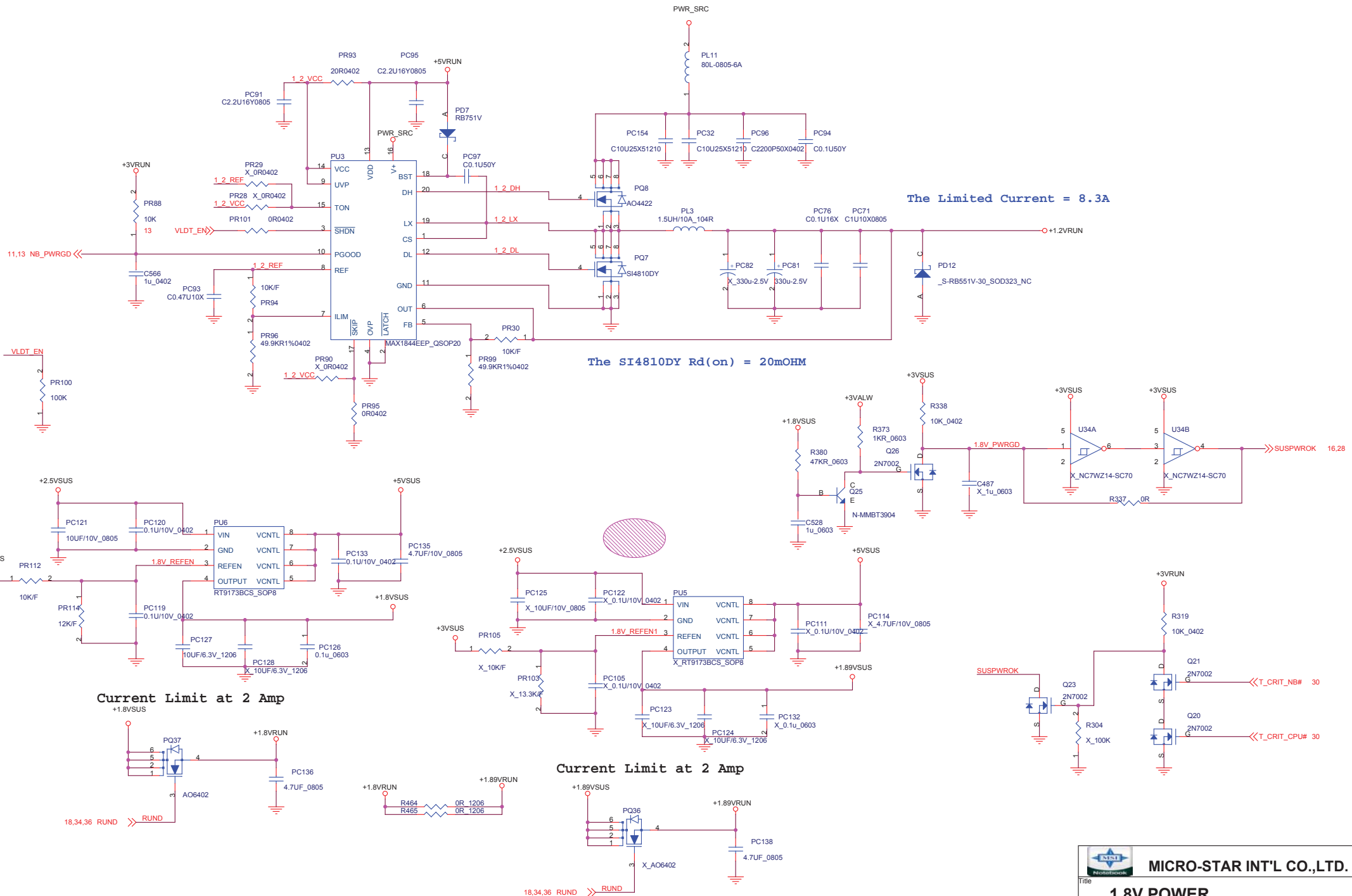
DHM_VCORE
LXM_VCORE
DLM_VCORE
DHS_VCORE
LXS_VCORE
DLS_VCORE

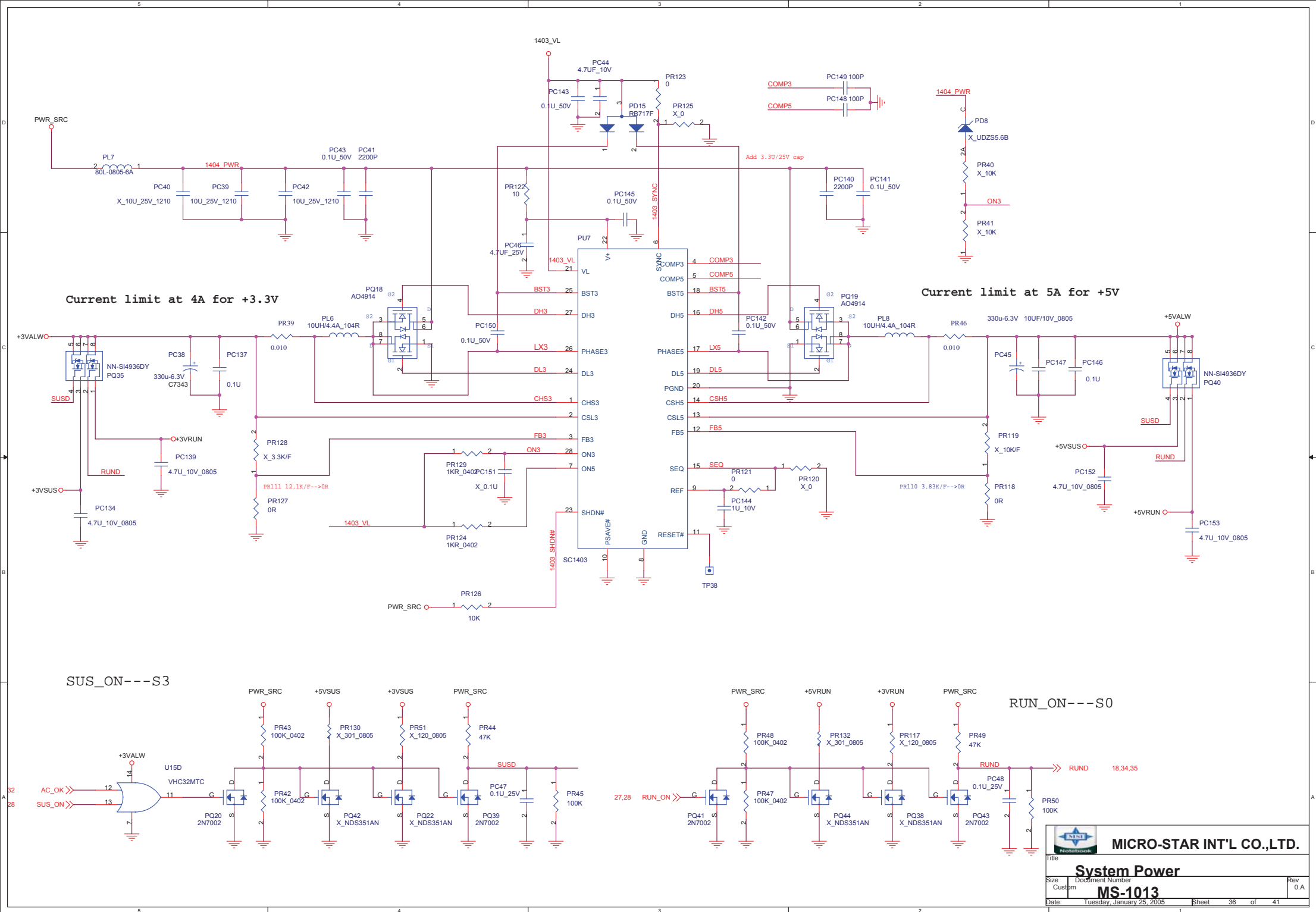
V I D					LPM VCORE
VID 4	VID 3	VID 2	VID 1	VID 0	v
0	1	0	0	0	1.250
0	1	0	0	1	1.225
0	1	0	1	0	1.200
0	1	0	1	1	1.175
0	1	1	0	0	1.150
0	1	1	0	1	1.125
.....					
1	1	0	1	0	0.800
1	1	0	1	1	0.775
1	1	1	0	0	0.750
1	1	1	0	1	0.725
1	1	1	1	0	0.700

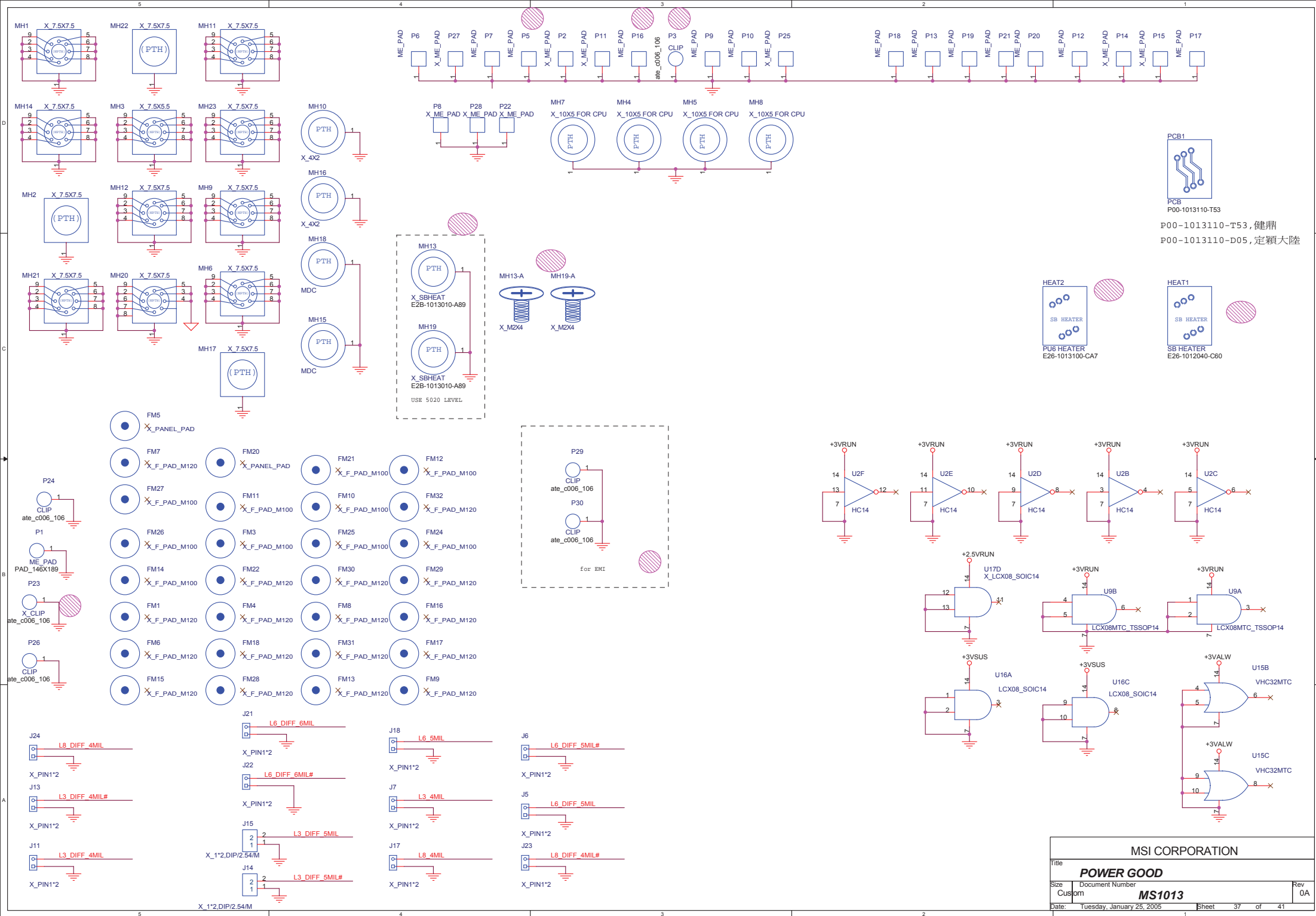
Current limit at 3.8A for SMDDR_VTERM

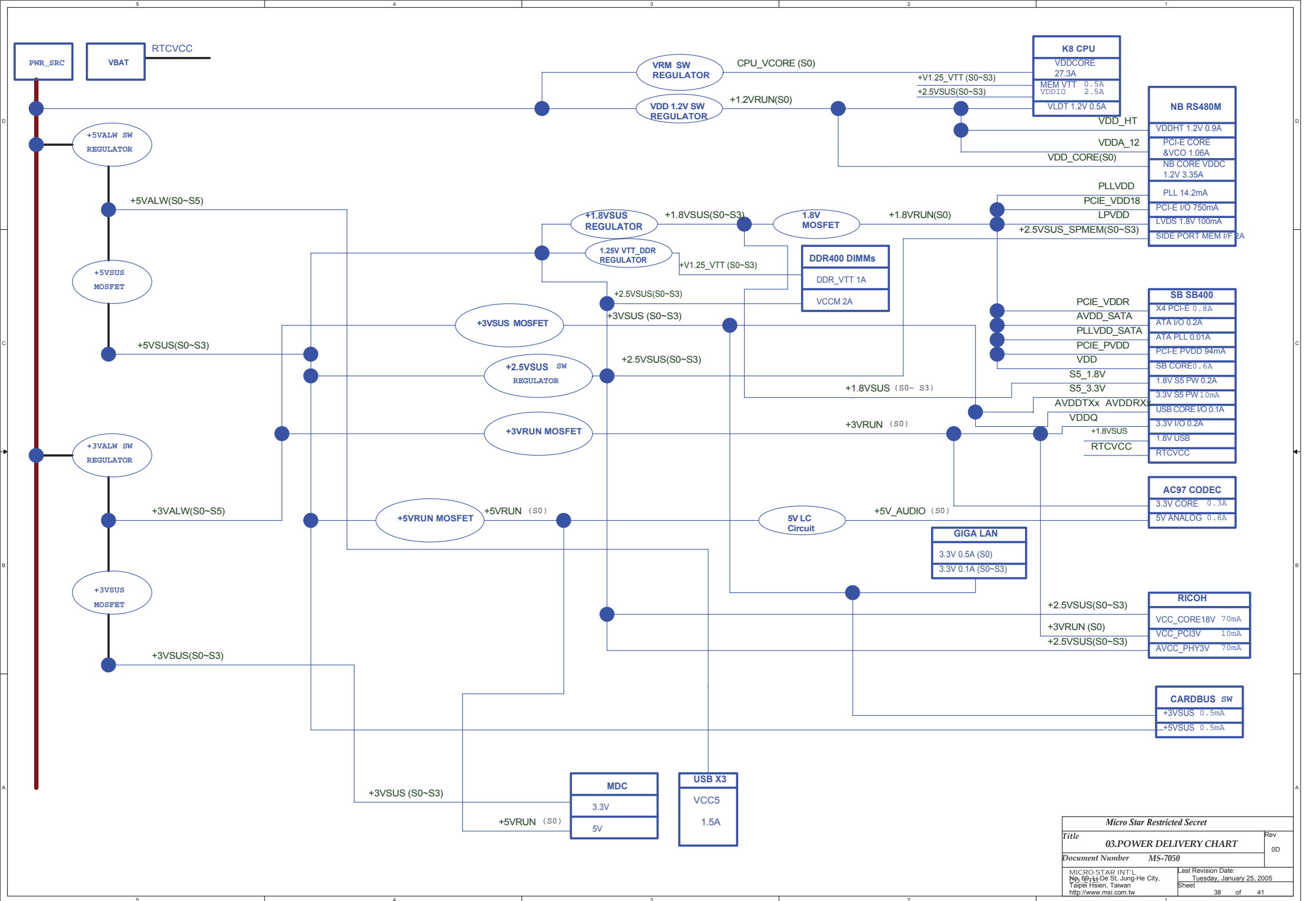
Current limit at 6A for +2.5VSUS



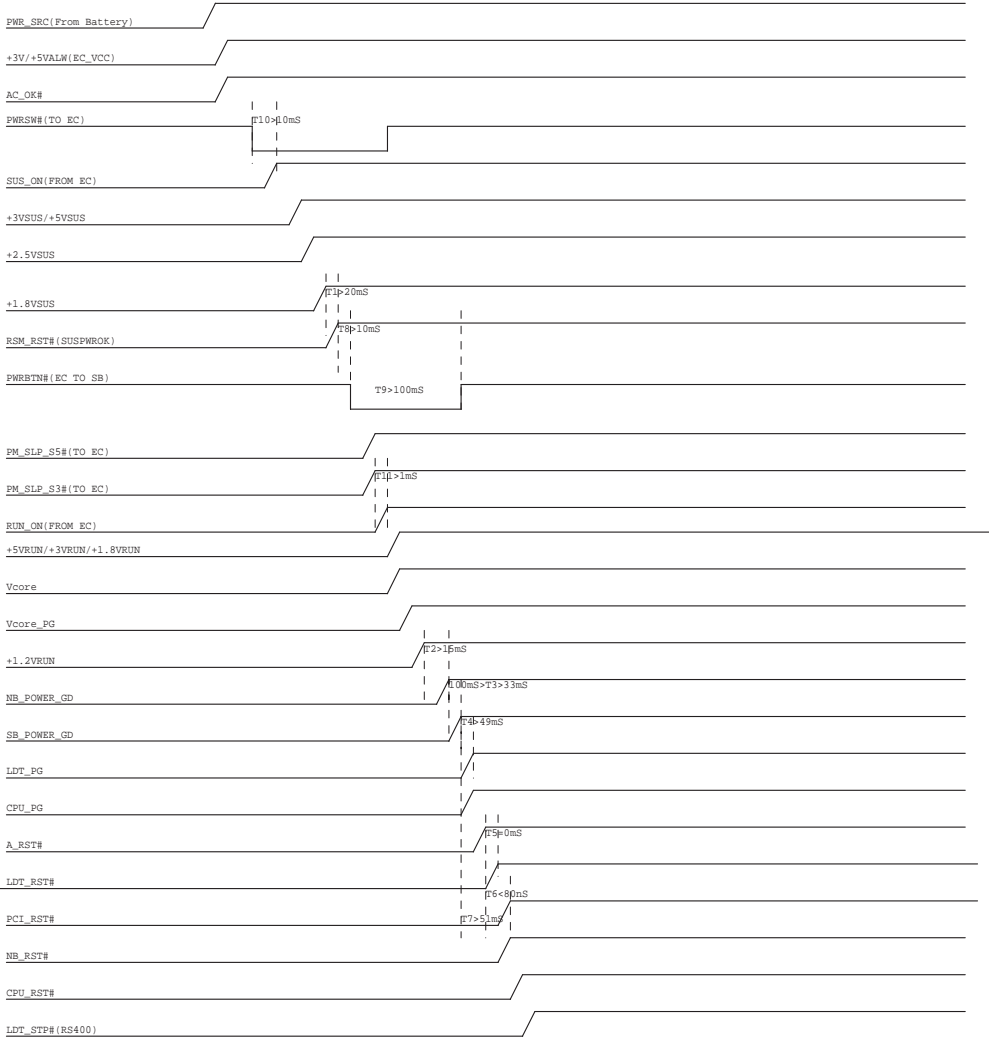




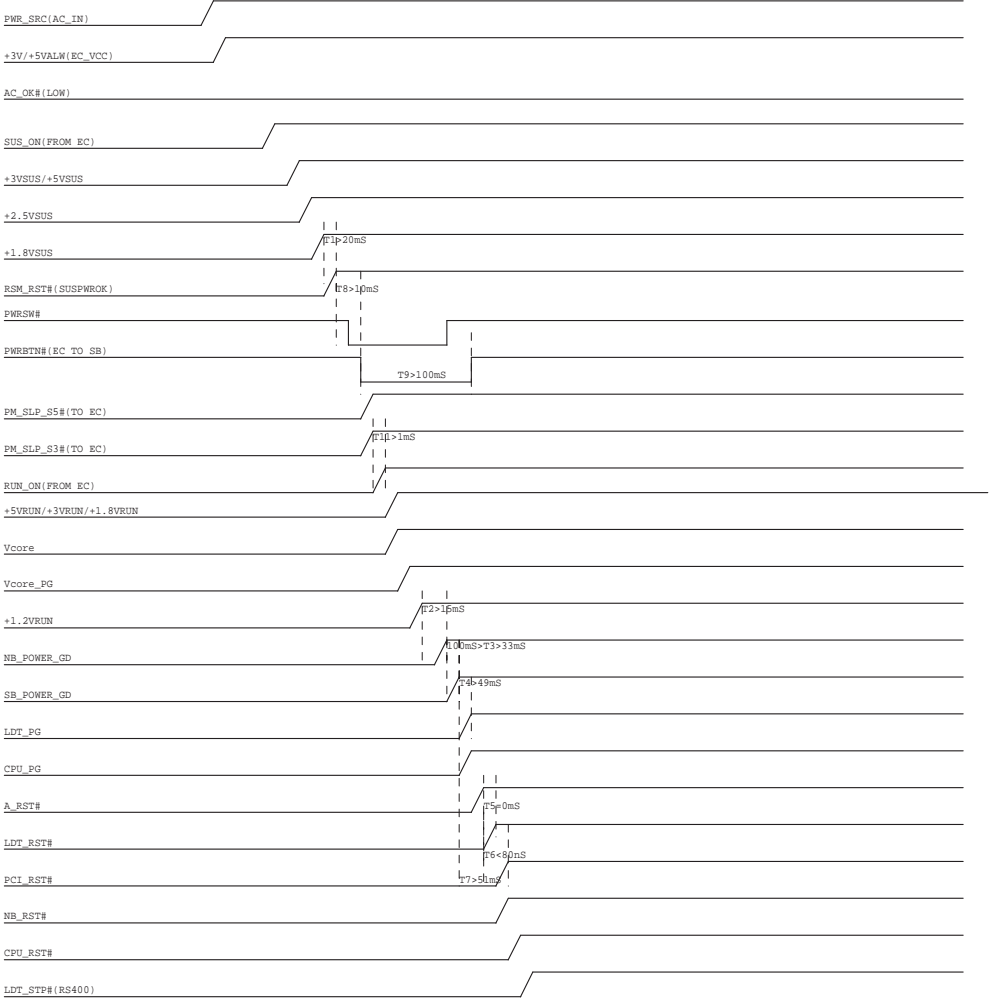


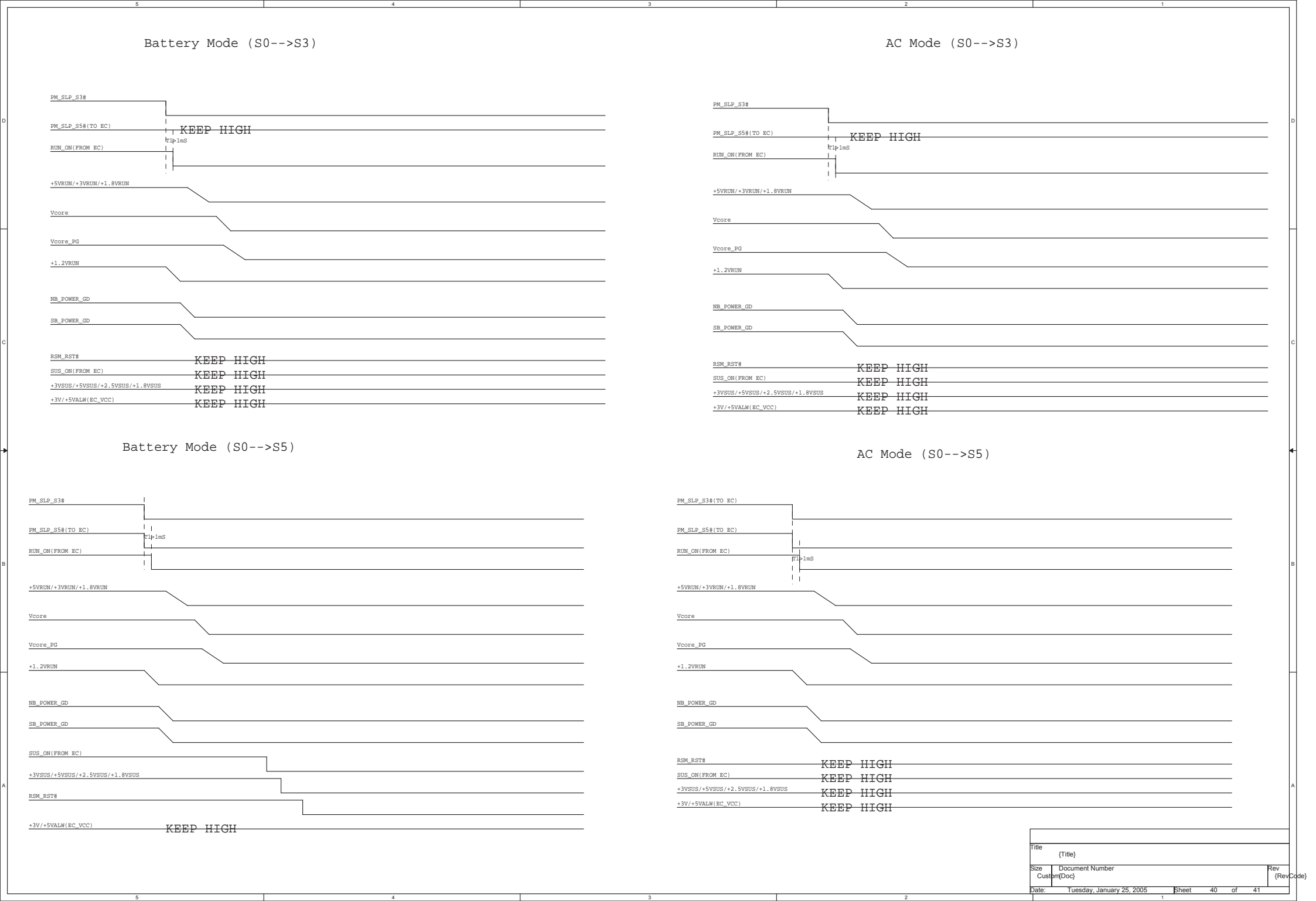


Battery Mode (S5-->S0)

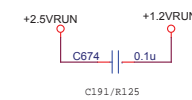
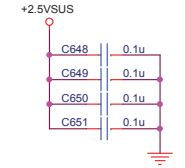
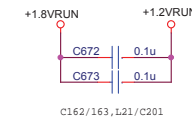
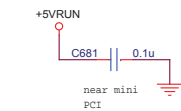
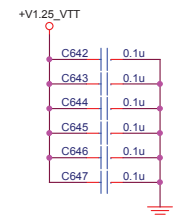
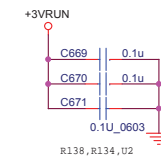
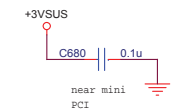
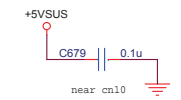
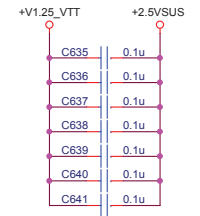
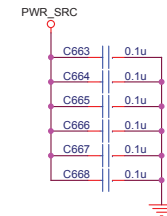
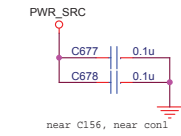
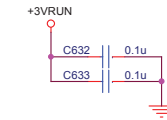
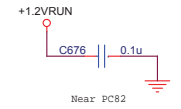
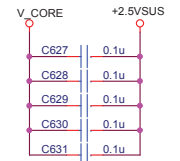
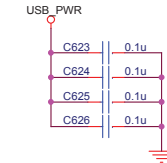
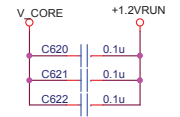
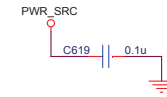
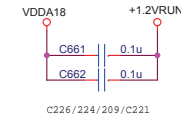
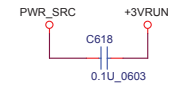
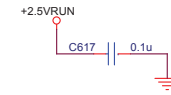
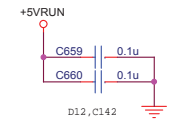


AC Mode (S5-->S0)





- 1.R136,R135 CHANGE TO 2.2K
- 2.CHANGE HWSPND# TO GPM5
- 3.POP R38, REMOVE R33 FOR POWER ON/OFF BACKLIGHT FLASH
- 4.L29,L27 CHANGE TO L02-6018024-T19 FOR EMI
- 5.PAGE 41 IS FOR EMI SOLUTION
- 7.R240-->0ohm for audio noise
- 8.add cpl4 for cdrom audio noise
- 9.add c566 for power sequence
- 10.CN4 pin9-10,pin11-12 for medion modem
- 11.C91,92,100,101,102,103,104,105,106,109,110,111,112,113,114 CHANGE TO 0402
- 12.C93,94,95,96,108,117,120,121,122 CHANGE TO 0402
- 13.PC62,63 change component for power team
- 14.PC64,66,69,PL4,PL1 change component,PC74,77,79 nonstuff for power team
- 15.PL6,PL8 change component for power team



NB_POWER_GD

SB_POWER_GD

SUS_ON(FROM EC)

RSM_RST#

Title		
{Title}		
Size	Document Number	Rev
Custom	(Doc)	(RevCode)
Date:	Tuesday, January 25, 2005	Sheet 41 of 41